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Analysis and design of two-device sensors with high-gain feedback enforced matching and linear digital output

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Analysis and design of two-device sensors with high-gain feedback enforced matching and linear digital output

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DEDICATION

To my friends and family.

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Even though it cannot read this, I want to thank my country, Argentina. Or maybe the people who make it what it is. Thanks to their fights we have high quality, free, and public education, and thanks to the effort of many, some of us can take advantage of this.

ABSTRACT

A technique to analyze and design different types of sensors and references is presented. Many well-known circuits, such as the bandgap reference, Widlar current reference and threshold-voltage-based temperature sensors, can be analyzed and modified thanks to the insight obtained with the method proposed. This systematic approach to the study of these circuits has the advantage of naturally leading to self-biased circuits, which are more insensitive to perturbations. High-gain feedback is employed to ensure matching of electrical variables of the circuit. This feedback loop allows embedding an Analog-to-Digital conversion as part of the system. As a result, a digital representation of the physical quantity of interest can be obtained. Moreover, this type of feedback loop is more flexible, since the controlled variable can be any kind of electrical parameter or design parameter that is controllable by a Digital-to-Analog circuit.

As an example of application, a variation of the Inverse Widlar temperature sensor is designed. By means of this technique, the sensor can be implemented without the need of devices with different threshold voltages, thus improving device matching. Also, the output is readily available as a digital code that is mathematically a linear function of the temperature to be measured.

CHAPTER I

INTRODUCTION

Sensing a physical quantity with a circuit relies on having one or more circuit components that are sensitive to this quantity and preferably, if possible, insensitive to other perturbations. In many cases a single component will not give such a performance, and the circuit around it tries to compensate for the errors. For example, a PN junction provides a very linear complementary to absolute temperature (CTAT) voltage that can be used to design bandgap references, but the linearity of this reference is not good enough to achieve a temperature stability of a few parts per million per ^{o}C [Tsivi80, SongB83, Rincon98, Malco01]. In that case, different kind of curvature correction circuits can be used to linearize the output. In a different situation, there are cases where the desired properties are obtained by the use of two of such components. Examples are the proportional to absolute temperature (PTAT) voltage obtained from a pair of PN junctions (also used in bandgap references), the Widlar current reference, which uses two devices to provide a constant-gm biasing, and the inverse Widlar temperature sensor, which uses two devices to generate an output voltage linear with the temperature [HeJun10, ZhaoC11, LeeSH11, ZhaoC13, WangYT13, WangYT15]. In each and every case, different terms that are not desired are eliminated from the output.

Using two devices to remove undesired terms and improve the properties of a single device seems promising. Analog design has been based on the similarities of two or more circuit components (so called matching) since almost its beginning. It is reasonable to expect that we can remove undesired effects of one circuit component by cancelling them out with similar contributions from a matched circuit component. Besides the possible new type of sensors that can be designed exploiting this concept, already existing sensors and references

can be understood under a different light. The interpretation of already existing circuits using a different perspective might shed some light on how to modify or improve them. That is, we can devise a design methodology that is not guaranteed to succeed but can provide new insights into the circuit being analyzed.

The technique presented in this work is not new. It appears naturally in many situations, particularly in sensors and references. What is interesting is the underlying principle that connects all these cases. Besides the examples of the bandgap reference, the Widlar current reference and the Inverse Widlar temperature sensor mentioned before, a literature review of sensors and references show that many circuits use ideas that are similar to the general principle described in this work. As examples, in [Roshan15] two MEMS (Micro Electro-Mechanical System) resonators are used together to improve the performance of a temperature sensor. In [Anand15], a temperature sensor based on the temperature variation of the threshold voltage of a MOSFET is designed. The authors rely on two oscillators to remove undesired terms and get a temperature measurement by taking the ratio of the output frequencies. Apart from sensors, voltage and current references have similar requirements when it comes to being insensitive to undesired physical variables and environmental or biasing changes. In [DeVita07], a low-power voltage reference is based on using two MOSFETs, in a similar way to the Inverse Widlar Structure.

In this work, a general framework for the analysis and design of the so called 'two-device sensor' is presented. The problem is divided in two parts, treated in Chapter 2 and Chapter 3 respectively. In Chapter 2, the concept of using two devices to obtain a sensor with improved performance is analyzed. A design procedure is sketched as in depth as possible for

a general case. To assist the explanation, and to give insight into the possibilities of the method, the three commonly used circuits mentioned before are used as examples.

In Chapter 3, the problem of realizing the conditions required in Chapter 2 to implement a two-device sensor is solved. It is shown that a two-device sensor architecture leads naturally to a self-biasing scheme. This is desirable, because self-biasing is a well-known technique used to reduce the sensitivity of the circuits to external variables. Also, the presence of a feedback loop gives the chance to embed an Analog-to-Digital conversion in the system, transforming the output of the sensor into a digital code without the need of any external conditioning amplifier and Analog-to-Digital Converter. Similar techniques have been used successfully in many works [Bakker96, Bakker02, Pertijs05, Perrott13, Heidary14, WengC15].

In Chapter 4, a temperature sensor based on the inverse Widlar circuit is designed. Using the concepts from previous sections, this temperature sensor includes a high-gain feedback loop to improve the matching of the devices. Also, this loop is implemented with a digital-to-analog converter, thus obtaining a digital output linear with the threshold voltage, and thus the temperature. The circuit is analyzed and designed, and simulation results are shown.

CHAPTER 2

TWO-DEVICE SENSOR

2.1 Definitions and Nomenclature

This section gives the definitions and explains the terminologies used throughout the document. Also, different examples are given, to aid the understanding.

In this work, a 'Device' is any component or circuit that is sensitive to a physical variable of interest or to be measured, such as temperature, magnetic field, mechanical stress or others. This physical variable under measurement is part of all the variables called 'Physical parameters':

- Physical parameter (P): Any physical quantity that affects the device property or operation, regardless there is interest on it or not. It is assumed that the two devices are subject to the same amount of these physical parameters (implicitly assuming they are nearby). A well-designed sensor will provide a linear response to changes in the physical parameter under measurement together with excellent insensitivity or rejection to variations in all other physical parameters.

The response of the device to the physical parameters is measured through the electrical variables on its terminals. These are called 'Electrical parameters':

- Electrical parameters (E): The electrical variables on the two or more terminals of each device. They can be voltage, current, frequency, period, delay, duty cycle, etc.

In general, these are quantities easily measurable and/or controllable by means of an electronic circuit.

The two devices used in designing a sensor in this work are of the same kind, but they are not equal. Being 'of the same kind' means that the two devices can be represented by the same equation (or system of equations) but some coefficients of this system of equations are different. The reason why the coefficients are different is because they have different 'Design parameters':

- Design parameters (Md): Quantities of a device set at the device design stage. Depending on the device type, these can be: width, length, and multiplicity in MOS transistors, emitter area and multiplicity in BJT, number of stages in a ring oscillator or delay line, etc. In general, the design parameters are variables that can be freely chosen by the designer. As a less traditional example, if the process being used has the option of high-threshold-voltage MOS transistors, then the use of low threshold voltage or high threshold voltage can be considered a design parameter. Even changing the length of the transistor provides a means to adjust the threshold voltage value, so it can be considered a design parameter. Furthermore a device does not need to be a single circuit component. For example, a PN junction with a resistor in series forms a device under the definition used here (not a single component, but a small circuit). The value of the resistor itself is a design parameter of this device. Under some conditions, even the biasing can be considered a design parameter, for example if the electrical parameters of interest are frequency, or duty

cycle, or small signal variations of the voltage or currents, and not large signal voltages and currents.

Finally, as said before, the device is modeled by an equation or system of equations. These have coefficients that can be chosen by the designer, and also have coefficients that are process dependent. These are called 'Process parameters' and complete the information needed to describe a device. An easy way to understand what they mean is to consider as process parameters those coefficients provided by the foundry as part of the component model, with the Process Design Kit (PDK):

- Process parameters (Mp): process dependent coefficients that form part of the model of the device. They are subject to process variations, long-term drift and matching errors. For example, in a MOS transistor the mobility is not a process parameter. Instead, the coefficients used in the MOS equation to describe the mobility are. For example, in the mobility expression $\mu = \mu_0(T/T_0)^{\eta_\mu}$, the process parameters are μ_0 and η_μ. The process parameters are the link between the physical parameters and the electrical parameters, so they are the key to measure a physical quantity. At the same time, they are responsible for the non-linear relations between them, and the changes with process variations. The success of a two-device sensor relies on cancelling out some of these process parameters and keeping some others. The better the matching between the two devices, the more similar the process parameters of the two of them are.

2.2 Use of Matching to Remove Undesired Terms

Using the parameters defined in the previous section, we can define a device by a system of equations that we can succinctly express as:

$$0 = d(E, P, M_P, M_D) \tag{2.1}$$

The equations defining a device determine the relation between the electrical parameters and the physical parameters. The coefficients of these equations are given by the design parameters, which can be controlled by the designer, and the process parameters.

A two-device sensor consist of two of such devices (named device A and device B throughout the rest of the document), with the same electrical parameters, and different design parameters. The physical parameters are assumed to be the same, and for now it is assumed that the process parameters are also the same (ideal matching). Under this definition, a two-device sensor is represented by the following system of equations:

$$\begin{cases} 0 = d(E, P, M_P, M_{DA}) \\ 0 = d(E, P, M_P, M_{DB}) \end{cases} \tag{2.2}$$

In Chapter 3, a method is described by which this system of equations can be implemented on a circuit level using feedback. It is clear that no advantage is obtained if the design parameters of device A and B are the same (that is to say, both equations in (2.2) are the same). Later on, some methods to determine which design parameters have to remain the same and which have to be different is presented.

Consider the case where some process parameters are undesired. For example, the mobility in MOS transistors has large temperature variations, or the gate capacitance has large

process variations, and is desirable to get rid of those if a temperature sensor is desired. A two-device sensor needs the property that the device equation can be split in two parts, such that the undesired parameters can be found only on one of them. First, the process parameters can be divided in undesired M_P^I and desired M_P^{II} as:

$$M_P = \{M_P^I, M_P^{II}\} \tag{2.3}$$

The device equation has to have the property that it can be expressed as:

$$0 = d(E, P, M_P, M_D) = d_I(E, P, M_P^I, M_D^I) - d_{II}(E, P, M_P^{II}, M_D) \tag{2.4}$$

This division also shows that some design parameters M_D^I are only on the first term. The way a two-device sensor will remove the undesired process parameters is by requiring that the design parameters M_D^I to be the same on both devices. This can be expressed as:

$$\begin{aligned} M_{DA} &= \{M_D^I\ , M_{DA}^{II}\} \\ M_{DB} &= \{M_D^I\ , M_{DB}^{II}\} \end{aligned} \tag{2.5}$$

Then, the system of equations from (2.2) can be written as:

$$\begin{cases} d_I(E, P, M_P^I, M_D^I) = d_{II}(E, P, M_P^{II}, M_{DA}) \\ d_I(E, P, M_P^I, M_D^I) = d_{II}(E, P, M_P^{II}, M_{DB}) \end{cases} \tag{2.6}$$

This system has a solution that only involves a subset of the process parameters. If the previous conditions can be achieved, there is a way to establish an equation that does not include the undesired process parameters M_P^I:

$$d_{II}(E, P, M_P^{II}, M_{DA}) = d_{II}(E, P, M_P^{II}, M_{DB}) \tag{2.7}$$

$$P = f(E, P, M_P^{II}, M_{DA}, M_{DB}) \tag{2.8}$$

Equation (2.8) is an explicit solution derived from (2.7). It shows that the physical parameters can be expressed a function of the electrical parameters, that can be controlled and measured, other physical parameters, a subset of the process parameters and the design parameters.

This derivation is rather general, so in the next sections specific examples are given. It has to be noticed that equation (2.8) is not necessarily an improvement over using a single device, but it forms the rationale behind this approach. For example, if the sensor is a temperature sensor, eliminating the mobility from the equation is a good starting point, if the objective is to obtain a linear measurement. It is also important that the equation relates the physical parameter with two parameters that the circuit can control: the electrical parameter and the design parameter. The relationship between physical parameters and electrical parameters is the initial requirement for a sensor. Having the physical parameter related to the design parameter is the door to use a Digital-to-Analog Converter (DAC) as part of the system, and then obtain a digital representation of the physical variable of interest.

2.3 Examples: The Widlar Pair and the PN Junction Pair

In this section, three well-studied circuits are analyzed: the PN junction pair that provides the PTAT reference in many bandgap voltage references, the Widlar current reference, and the inverse Widlar temperature sensor. The analysis is intended to show how the concept of two-device sensor is applied in those cases. Later on in this work the inverse Widlar temperature sensor is analyzed in detail and variations of the original implementation are shown.

The PN junction pair

The PN junction device, in this case, is defined as a junction with an area of size A, series connected with a resistor of value R, as shown in the next figure. A voltage V is applied to the device, and a current I flows through it.

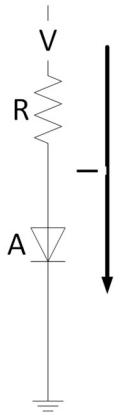

Figure 1 - PN junction device

In this device we can identify the electrical parameters as the terminal voltage and the current. The design parameters are the junction area and the resistor value. The physical

parameter is the temperature. The process parameters are all the coefficients shown in the next device equations (2.10) and (2.11):

$$V = V_{Junction} + V_R \tag{2.9}$$

$$V = \frac{kT}{q}\ln\left(\frac{I}{I_S}\right) + I \cdot R \tag{2.10}$$

with:

$$I_S = \frac{qAn_i^2\overline{D}}{N_B} \tag{2.11}$$

where q and k are constants, electron charge and Boltzmann constant respectively. n_i is the intrinsic carrier concentration, $\overline{D}$ is the effective minority carrier diffusion constant, both with temperature dependence, and N_B is the Gummel number, representing the total number of impurities per unit area in the base, which suffers from process variations. The resistor is assumed to be ideal (no process parameters on it, only a single design parameter), to simplify this analysis. As can be noticed, many of the process parameters depend on process variations and introduce complex, nonlinear temperature dependency.

When used to generate a PTAT reference (current reference, in this case), two of these type of devices are used [Tsivi80], and some external circuit forces them to have the same electrical parameters, i.e. same current and same voltage. The system of equations can be written as:

$$\begin{cases} V = \dfrac{kT}{q}\ln\left(\dfrac{I}{I_{SA}}\right) + I \cdot R_A \\ V = \dfrac{kT}{q}\ln\left(\dfrac{I}{I_{SB}}\right) + I \cdot R_B \end{cases} \tag{2.12}$$

Notice that this set of equations in (2.12) is specific to the PN junction devices, and it is in the form of the general set of equations given in (2.2). In this case, our interest is the relation between the current and the temperature. Solving for the current gives:

$$I = \frac{1}{R_A - R_B}\frac{kT}{q}\ln\left(\frac{A_A}{A_B}\right) \tag{2.13}$$

This current has no dependency on any of the undesired process parameters, as expected. This is a good place to look at why this is possible: the equation of this device can be split as required by (2.4). This is shown next:

$$0 = d(E, P, M_P, M_D) = V - \frac{kT}{q}\ln\left(\frac{I}{I_S}\right) - I \cdot R \tag{2.14}$$

$$d_I(E, P, M_P^I, M_D^I) = V - \frac{kT}{q}\ln\left(\frac{I \cdot N_B}{q n_i^2 \overline{D}}\right) \tag{2.15}$$

$$d_{II}(E, P, M_P^{II}, M_D) = \frac{kT}{q}\ln(A) - I \cdot R \tag{2.16}$$

Since this is possible, the first term d_I gets cancelled out, and the second term d_{II}, with no dependency on undesired process parameters, stays.

The Widlar current reference

A Widlar current reference gives a current with some particular dependency on the mobility, which makes it useful to have a constant-gm biasing. Similarly as with the PN junction, a more general case is analyzed, which can be reduced to the traditional case. Consider the following device:

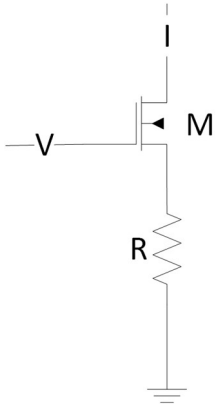

Figure 2 - Degenerated MOSFET

Notice that, for this derivation, only two electrical variables are considered, even though the device has a drain voltage, which represents a third electrical variable. It is considered that it is high enough to keep the device in the saturation region, and that its value will not affect the equation (i.e. channel length modulation and velocity saturation are neglected). Also, strong inversion and square law model are assumed. The device equation is:

$$V = \sqrt{\frac{2I}{\mu C_{ox} M}} + V_T + IR \tag{2.17}$$

The electrical parameters are the gate voltage and the drain current (the drain voltage is neglected for simplicity, as said before). The design parameters are the device size $M =$

W/L, and the resistance R. According to the definition of process parameters, the mobility, and the threshold voltage are expressed in terms of other more fundamental parameters. For a very simple MOSFET model, they can be expressed as:

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{\eta_\mu} \tag{2.18}$$

$$V_T = V_{T0} - \alpha(T - T_0) \tag{2.19}$$

In this model, the process parameters are $\mu_0, \eta_\mu, V_{T0}, \alpha$, and not the mobility or the threshold voltage themselves. The only physical parameter present on the model is the temperature. In the case of the Widlar current reference, the objective is not to obtain a temperature sensor. Instead, a mobility extraction is desired. By using two of these devices, the next system of equations is formed:

$$\begin{cases} V = \sqrt{\dfrac{2I}{\mu C_{ox} M_A}} + V_T + IR_A \\ V = \sqrt{\dfrac{2I}{\mu C_{ox} M_B}} + V_T + IR_B \end{cases} \tag{2.20}$$

If the conditions $R_B > R_A$, and $M_B > M_A$ are fulfilled, the solution for the current is:

$$I = \frac{2}{(R_B - R_A)^2 \mu C_{ox} M_{EQ}} \tag{2.21}$$

With:

$$M_{EQ} = \left[M_A^{-1} + M_B^{-1} - 2(M_A M_B)^{-1/2}\right]^{-1} \tag{2.21}$$

The use of this result can be noticed once this current is used to current-bias another MOSFET. In that case, the transconductance of that transistor, assuming it is in strong inversion, is ideally temperature and process independent, except for the dependency on the resistor value, as shown in equation (2.22). This result is particularly useful to bias differential pair, because the unitary-gain frequency depends on this transconductance.

$$g_m = \frac{2}{R_B - R_A}\sqrt{\frac{M}{M_{EQ}}} \tag{2.22}$$

The Inverse Widlar temperature sensor

In a similar way as the previous circuit extracts mobility, this circuit extracts the threshold voltage of a MOS transistor. As shown in equation (2.19), the threshold voltage is expected to be linear with temperature, and a measurement of the threshold voltage can be used to measure temperature. The device, in this case, is just a MOSFET, if the process has the option to choose between low and high threshold voltages, or if different lengths are used to cause different threshold voltages. If not, two MOSFET can be stacked up to generate the same effect of threshold voltage change, as shown:

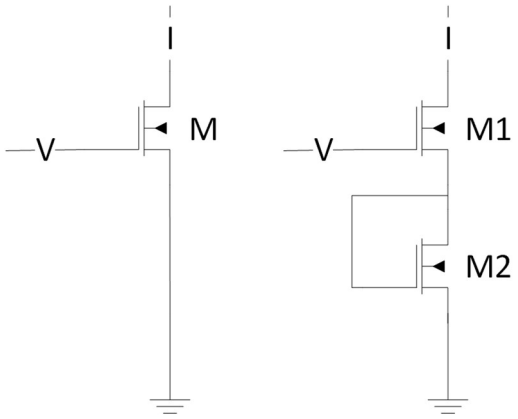

Figure 3 - Two options for a MOSFET with selectable threshold voltages

For the single MOSFET, the device equation is:

$$V = V_T + \sqrt{\frac{2I}{\mu C_{ox} M}} \tag{2.23}$$

It is simple to show that for the device with stacked MOSFETs the device equation is:

$$V = 2V_T + \sqrt{\frac{2I}{\mu C_{ox} M_{EQ}}} \tag{2.24}$$

With:

$$M_{EQ} = \left[M_1^{-1/2} + M_2^{-1/2}\right]^{-2} \tag{2.25}$$

Either in a process with multiple threshold voltages or a process with a single threshold voltage, a high-threshold voltage MOSFET can be obtained. So, this option is considered as a

design parameter in the inverse Widlar sensor. In the two device inverse Widlar sensor, the device A uses a low threshold voltage, while the device B uses a high threshold voltage. The system of equations for this case is:

$$\begin{cases} V = V_{TA} + \sqrt{\dfrac{2I}{\mu C_{ox} M_A}} \\ V = V_{TB} + \sqrt{\dfrac{2I}{\mu C_{ox} M_B}} \end{cases} \tag{2.26}$$

Define and apply the condition $\chi = \sqrt{M_A/M_B} < 1$, and also $V_{TB} > V_{TA}$, then the voltage is:

$$V = \frac{1}{1-\chi}(V_{TB} - \chi V_{TA}) \tag{2.27}$$

This voltage is a linear combination of the threshold voltages, which in turn are linear with temperature. The only coefficient in the expression is a ratio of device sizes, which is temperature and process independent. The mobility, which causes large and non-linear temperature dependency, and the gate capacitance, which causes process dependency, are not present in equation (2.27). The same as before, the reason why this is possible is because the device equation of (2.23) or (2.24) can be split as in equation (2.4), as shown:

$$0 = d(E, P, M_P, M_D) = I - \frac{1}{2}\mu C_{ox} M (V - V_T)^2 \tag{2.28}$$

$$d_I(E, P, M_P^I, M_D^I) = \frac{2I}{\mu C_{ox}} \tag{2.29}$$

$$d_{II}(E, P, M_P^{II}, M_D) = M(V - V_T)^2 \tag{2.30}$$

These three examples are intended to show how to use the different definitions. But how to apply the conditions to the device equation, in order to be able to cancel out an undesired process parameter is not obvious. The next section analyzes specific cases and derives the corresponding conditions. These conditions determine which design parameters have to be the same on both devices and which have to be different. Probably, the most important concept is that a device is not a fixed component. For example, if there is a need to modify the threshold voltage of a MOSFET, there are many different ways to do so: using a high-threshold voltage device when available in the process, stacking two MOSFETs, having different lengths, or adding extra components to generate the effect of having an effective threshold voltage that is different than the actual threshold voltage. By analyzing the device equations, the designer can understand in which places changes are needed and how to design a new device accordingly.

2.4 Conditions to Remove Different Types of Terms

This section analyzes the conditions imposed over a two-device sensor needed to eliminate the dependency of the electrical parameters on some process parameters. The case analyzed is a device with only one terminal, and the electrical parameters are the voltage and the current in that terminal. The system of equations of (2.2) is repeated here as (2.31) for convenience:

$$\begin{cases} 0 = d(E, P, M_P, M_{DA}) \\ 0 = d(E, P, M_P, M_{DB}) \end{cases} \tag{2.31}$$

Each of these equations establish a relation between the voltage and the current of each device. Since the design parameters are different, the relations are different. Then, the system can be expressed as:

$$\begin{cases} I_A = f_A(V_A) \\ I_B = f_B(V_B) \\ I_A = I_B = I \\ V_A = V_B = V \end{cases} \tag{2.32}$$

Graphically, the solution of the system of equations is the set of points (V, I), where the two I-V curves for device A and device B intersect, as shown in the next figure with only one solution or I-V curve intersection:

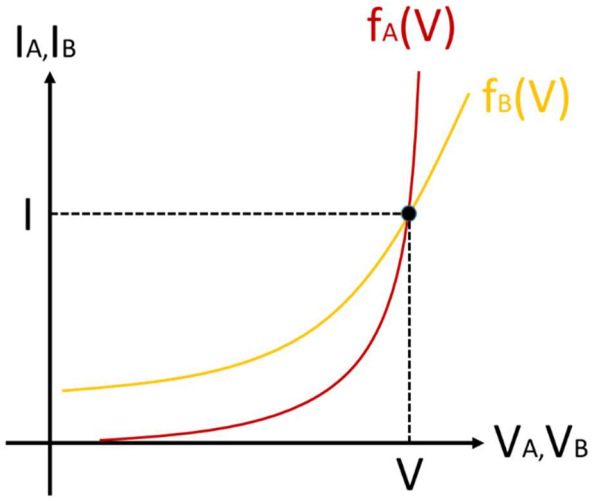

Figure 4 - Solution of the system as intersection of the functions of each device

The system of equations might have more than one solution, and which of those is the actual solution of the system is a startup issue [WangYT12], which is covered in more detail in Chapter 3. It is interesting to note that this type of system of equations is characteristic of self-biased circuits. The solution is defined by the intersection of two curves, and these are the ones that determine the values of the operating voltages and the currents.

The solution of the system does not tell much about how to make it independent of certain process parameter. Also, it requires finding that solution first, which is not trivial (many device equations are transcendental, for example). Instead of analyzing the solution, the system of equations from (2.32) can be analyzed directly. Since the objective is to make at least one of the electrical parameters independent of a specific set of process parameters, a differential analysis can give enough information. The system of equations from (2.32) satisfies the following system of differentials:

$$\begin{cases} \Delta I = \dfrac{df_A}{dV}\Delta V + \dfrac{df_A}{dP}\Delta P + \dfrac{df_A}{dM_P}\Delta \mathrm{M_P} \\ \Delta I = \dfrac{df_B}{dV}\Delta V + \dfrac{df_B}{dP}\Delta P + \dfrac{df_B}{dM_P}\Delta \mathrm{M_P} \end{cases} \tag{2.33}$$

Note that the differentials in both equations are the same. By definition, physical parameters and process parameters are the same for both devices, and the structure of a two-device sensor forces the electrical parameters of both devices to be the same. The design parameters are implicit in the fact that the functions of each device are slightly different, and so are their derivatives.

Suppose there is a change on a physical parameter. The solution of the system moves away, as shown on the next figure:

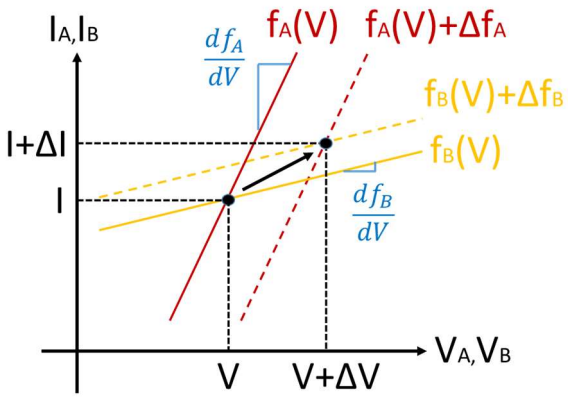

Figure 5 - Change on the solution when a physical parameter changes

The change in either the voltage or the current can be computed by solving equations (2.33), which is a system of linear equations:

$$\Delta V = \frac{\frac{df_B}{dP} - \frac{df_A}{dP}}{\frac{df_A}{dV} - \frac{df_B}{dV}} \Delta P \tag{2.34}$$

The conclusion that can be derived from this result is that, if the parameter is undesired (it belongs to M_P^I), the way to become independent of it, at least locally, is by forcing the next equality:

$$\frac{df_B}{dP} = \frac{df_A}{dP} \tag{2.35}$$

In general, these derivatives will depend on a subset of the design parameters. The way to make these derivatives equal is by making those design parameters the same. That is, they should belong to the subset of design parameters M_D^I.

It is clear that this condition is easier to fulfil if the two devices are of the same kind, because the functions are alike. If the two devices were too different, it would be more difficult or sometimes impossible to make these derivatives equal. Here lies the strength of the two-device sensor approach.

Techniques to remove the dependency on undesired parameters

In the previous subsection it was shown that the requirement for an electrical variable to be independent of a given parameter (either physical or process) is that both devices have the same derivative with respect to that parameter. In this section, some common cases are analyzed. Without loss of generality, it is assumed here that the objective is to make the voltage V insensitive to a (physical or process) parameter called μ. Different situations in which μ might appear are analyzed, in order to find out what are the requirements imposed on the devices.

In general, a single device will have an equation like (2.36), where $f(\cdot)$ is also function of the design parameters and expected to be different in the two devices:

$$I = f(V) \tag{2.36}$$

Multiplicative case

The equation (2.36) takes the form:

$$I = \mu \cdot g(V) \tag{2.37}$$

When multiplicative factors are present, logarithmic differentiation gives the same information in an easier way:

$$\frac{dln(I)}{d\mu} = \frac{1}{\mu} \tag{2.38}$$

This result means that if the undesired parameter is multiplicative, using a two-device sensor will always get rid of it, independently of the design parameters. This is true, because both devices will have the same derivative (2.38), and it does not include any function of the design parameters. An example of this case is the mobility and gate capacitance in the inverse Widlar temperature sensor, and the saturation current in a PN junction PTAT generator. The next equation shows that both the mobility and the gate capacitance are multiplicative factors in the MOSFET equation:

$$I = \frac{1}{2}\mu C_{ox} M(V - V_T)^2 \tag{2.39}$$

Additive case

The equation (2.36) takes the form:

$$I = [\mu + g(V)] \cdot h(V) \tag{2.40}$$

And the derivative is:

$$\frac{dI}{d\mu} = h(V) \tag{2.41}$$

In order for a two-device sensor to cancel this undesired parameter, both devices should give the same value in $h(V)$ when evaluated with the solution of the system (2.31). One way to achieve this is by forcing $h(V)$ to be the same function in both devices for any value of V by making the design parameters present on it the same, although this is not a necessary condition. An example of this case is the expression for the Widlar current reference. It is insensitive to the threshold voltage, and its expression is shown next, where the function $h(V) = 1$:

$$V = V_T + \sqrt{\frac{2I}{\mu C_{ox} M}} + IR \tag{2.42}$$

Exponential case

The equation (2.36) takes the form:

$$I = g(V) \cdot [h(V)]^{\mu} \tag{2.43}$$

Using logarithmic differentiation:

$$\frac{dln(I)}{d\mu} = \ln[h(V)] \tag{2.44}$$

In this case, the requirement is that the base of the exponential to be the same on both devices, when evaluated at the solution of (2.31). As before, a sufficient condition is to make them the same for every possible voltage value, forcing the design parameters present on $h(V)$ to be the same, but the condition is not necessary.

Power case

The equation (2.36) takes the form:

$$I = g(V) \cdot \mu^{h(V)} \tag{2.45}$$

Using logarithmic differentiation:

$$\frac{dln(I)}{d\mu} = \frac{h(V)}{\mu} \tag{2.46}$$

Similarly to the previous case, the exponent, in this case, has to be the same on both devices, when evaluated at the solution of (2.31).

CHAPTER 3

SYSTEM-LEVEL IMPLEMENTATION

3.1 Use of Feedback to Solve the Equations

In Chapter 2, it is explained how using two similar (but not equal) devices helps to cancel the dependency of electrical parameters on undesired process or physical parameters. The assumption was that there is a way to force all the electrical parameters to be the same between the two devices. This chapter details a possible solution to that requirement.

The case analyzed is when the devices have two electrical parameters that are required to be equal. For now, they are called voltage and current, but this can be extended to other types of electrical parameters, as frequency, delay, or duty cycle. Consider the case of two two-terminal devices shown next:

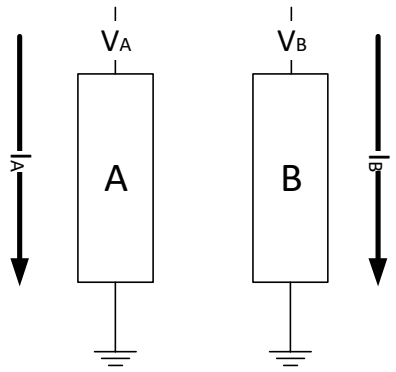

Figure 6 - Generic two-terminal devices

The condition that has to be fulfilled is:

$$\begin{cases} V_A = V_B \\ I_A = I_B \end{cases} \tag{3.1}$$

Using a feedback loop, one set of variables can be measured and tested for equality, while the remaining are controlled to force the first ones to be equal. In the simple case considered, two possible solutions are:

- Voltage mode: Apply the same voltage to both devices and measure the current difference. Adjust the applied voltage until the currents are equal.
- Current mode: Inject the same current into both devices and measure the voltage difference. Adjust the injected current until the voltages are equal.

Among different ways that two voltages can be made the same, the most straightforward way is by connecting those two nodes together (i.e. parallel connection). A slightly different approach can be used for the currents. Even though a series connection would force the currents to be the same, in circuit design, it is more convenient to force device currents to be the same by biasing them with copies of the same current mirror.

When both currents and voltages are forced to be the same, there is only a limited set of points of the form (V, I) that will survive those requirements. Those are the solutions of the system of equations of the two-device arrangement. The next figure shows the process by which a 'voltage mode' feedback loop forces the currents to be the same, and thus finds one solution of the system. It is assumed that the system starts from a voltage V_1, and the currents on the two devices are different. The feedback loop senses the currents and increases the voltage to the value V_2. Since the currents are still different, the process continues until finally reaching the voltage V_3, where the currents are equal. Note that this is a simplified explanation

that is not concerned about the true dynamic of the loop along the time. The intention is to show how a feedback loop 'solves the system of equations'.

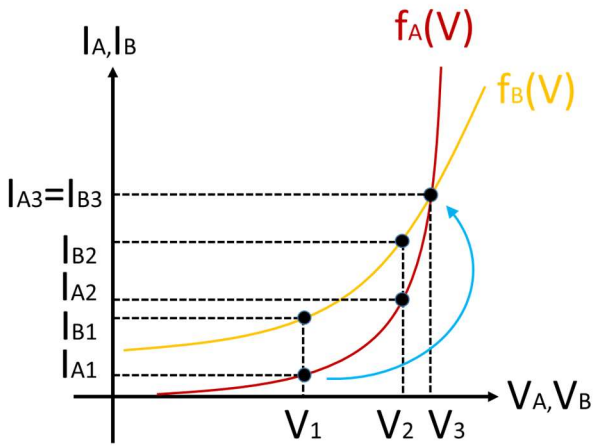

Figure 7 - Voltage mode feedback loop dynamic

A voltage mode feedback loop requires sensing the currents of the devices and comparing them with an error amplifier. The output of the error amplifier, in turn, controls the voltage. A block level representation is shown in the next figure:

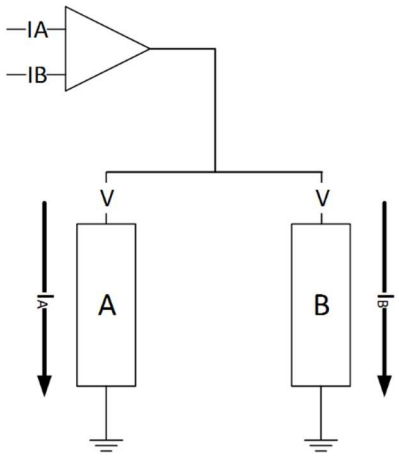

Figure 8 - Voltage mode feedback loop diagram

A current mode feedback loop seems more natural from an analog design perspective. It requires sensing the voltage difference between the devices, and controlling the current injected into both of them. The next figure shows a possible implementation:

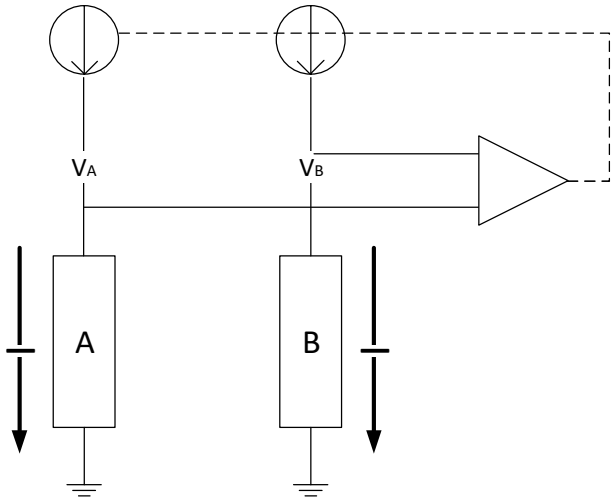

Figure 9 - Current mode feedback loop diagram

Notice that these two solutions lead themselves to a self-biased circuit. There is no external reference, and there is no way to know what the voltages or currents are, unless the system of equations is solved, or explicit measurement units are used to measure these.

DC Stability and the startup problem

It can be said that the problem of solving the system of equations has been put on the hands of the feedback loop. It will try and find the voltage (current) that makes the current (voltage) difference to be small enough, ideally zero. Since the device equations are non-linear, the question that remains to be answered is how to guarantee that the solution found is the

desired solution. This is the same as the traditional startup problem of self-biased circuits [WangYT12].

The error amplifier will measure the difference between the currents (voltages) and decide whether the output voltage (current) should be increased or decreased. This can be represented by the following block diagram:

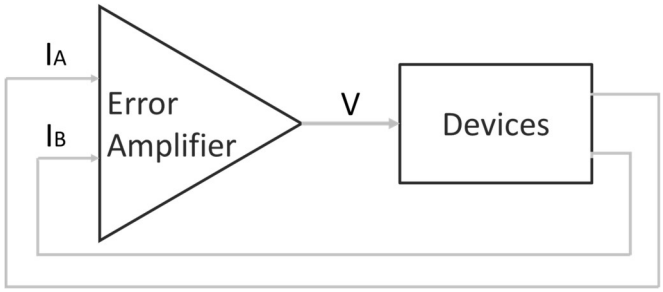

Figure 10 - Voltage mode feedback loop block diagram

The devices can be characterized by the relationship between the voltage applied and the error in the currents (or current difference), as:

$$\Delta I = I_A - I_B = f_A(V) - f_B(V) \tag{3.2}$$

The expression (3.2) can have more than one zero. Depending on the sign of the error amplifier gain, some of them are stable solutions and some are unstable solutions. The next figure shows an artistic representation of what the devices transfer function could be. In fact, an inverse Widlar temperature sensor shows transfer functions that look like this.

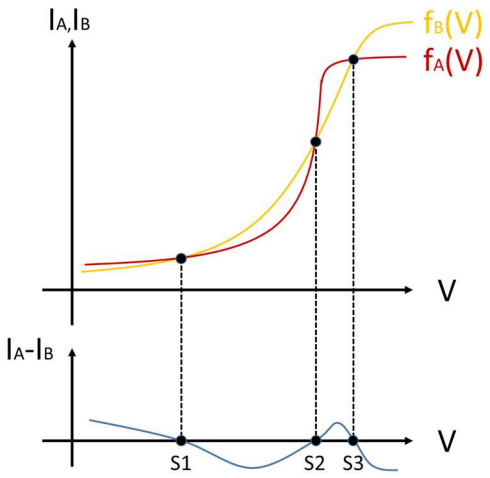

Figure 11 - Example of device functions, showing multiple zeros

In Figure 11 three solutions, labeled S1, S2, and S3 are found. Depending on the sign of the gain of the error amplifier, either S2 is stable, or both S1 and S3 are stable. The next figure shows how the voltage evolves on each case, and reaches a stable solution:

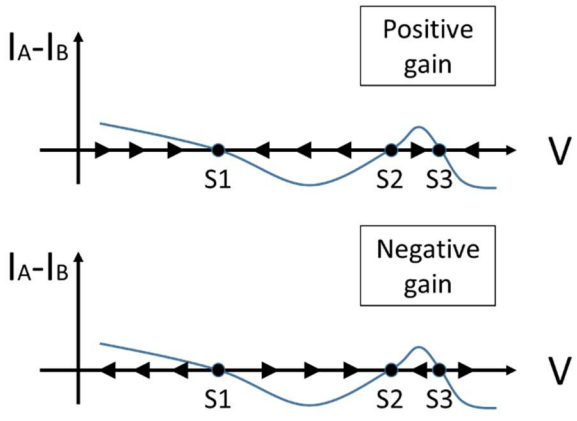

Figure 12 - Stable and unstable solutions depending on the sign of the error amplifier's gain

For example, if the desired solution is S2 (it corresponds to the saturation region in the inverse Widlar sensor), the error amplifier gain has to have negative sign. If the voltage starts

between S1 and S3, it will converge to S2. But if it starts to the left of S1, or to the right of S3, it will diverge and eventually hit one of the power rails and stay there. Startup circuits are used to avoid this scenario by modifying the circuit such that S1 and S3 are beyond VSS and VDD, and therefore the entire voltage range [VSS, VDD] is always inside the zone that converges to the desired solution S2. Alternatively, the startup issue in the above two-device sensor can be addressed in conjunction with the error amplifier design by clamping the output of the error amplifier in such a way that it always stays in a smaller desired region around S2 that is strictly inside the region of convergence between S1 and S3. This issue will be covered later on, when dealing with a specific implementation of the temperature sensor in Chapter 4.

3.2 Feedback with Boolean Output

In many situations, the output of a sensor is further processed by a digital system. A typical way in which the conversion is implemented is shown next figure in which the sensor is followed by a conditioning amplifier and an Analog-to-Digital Converter (ADC):

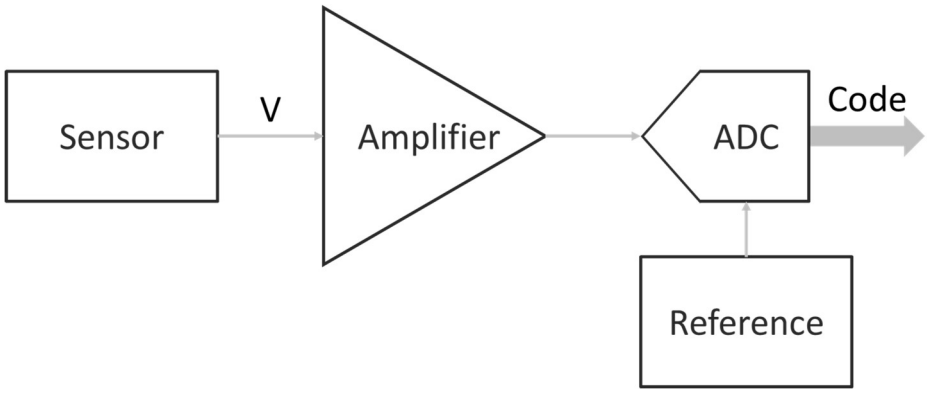

Figure 13 - Traditional sensor front-end

In this approach, the output of the sensor is fed into a conditioning amplifier, which takes it to an appropriate DC level with suitable amplitude and bandwidth to be quantized. Then, the signal is digitized using an ADC, and the output is sent to the digital system.

A different approach can be used by noticing that a two-device sensor requires the presence of a feedback loop, and that many ADCs are based on using a DAC in a feedback loop to convert the input signal. Such ADCs include Successive Approximation ADC (SAR ADC), Sigma-Delta ADC, or tracking ADC. Concrete examples of Sigma-Delta ADCs following similar approaches can be found in [Bakker96, Bakker02, Pertijs05, Perrott13, Heidary14, WengC15]. Motivated by these observations, the proposed structure for a two-device sensor will use a DAC in the Boolean feedback loop as shown below:

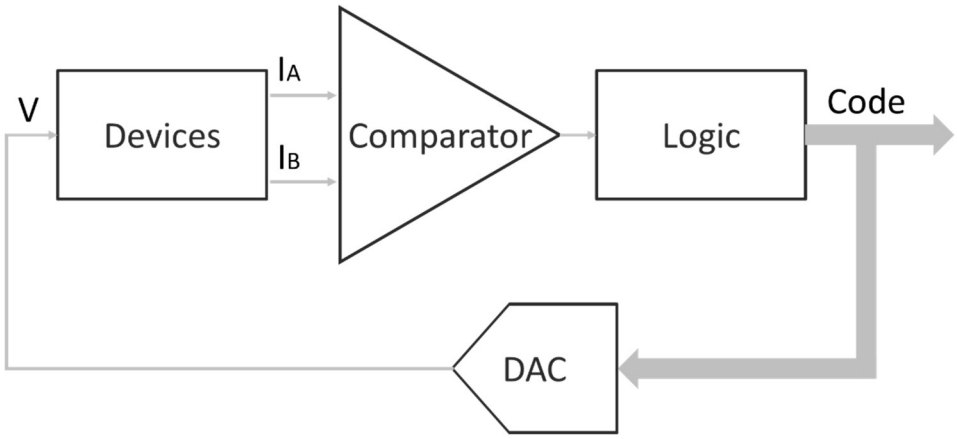

Figure 14 - Two-device sensor with boolean feedback

Comparing Figure 10 and Figure 14, it can be noticed that the error amplifier has been replaced by three blocks: a comparator, a block with logic and state machines, and a DAC. It can be said that these three, together, form a mixed-signal error amplifier. This error amplifier not only closes the loop of the two-device sensor, but also provides an output code that is a

digital representation of the electrical parameter controlled (a voltage in the figure). The structure as shown in Figure 14 suits very well SAR ADCs and tracking ADCs. For a Sigma-Delta ADC, some special considerations are needed, which are not discussed in this work.

As an example, assume the logic block is configured to perform a binary search, as in a SAR ADC. The devices have the transfer functions shown in Figure 11, and it is assumed that the DAC's output is limited to the range between the zeros S1 and S3 (this is one way in which a startup problem can be avoided). The next figure shows the binary search for the first three bits:

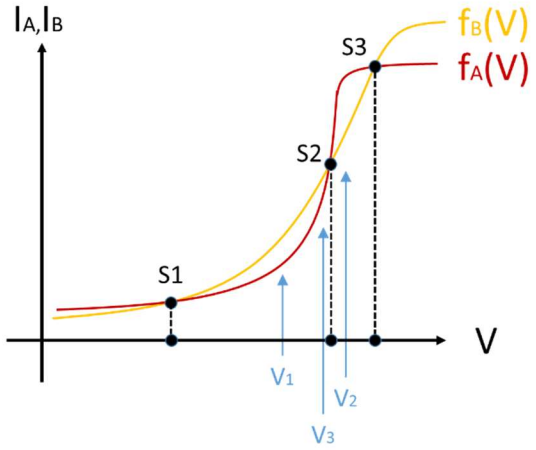

Figure 15 - Binary search for a two-device sensor, performed by the SAR logic

The steps are the same as in the SAR ADC, and in this case they are:

1) Set the output of the DAC to the middle of search range (V1)
2) Read comparator output: Because $I_A < I_B$, the output is zero. Move the output up by one quarter of the range (V2)
3) Read comparator output: Because $I_A > I_B$, the output is one. Move the output down by one eighth of the range (V3)

4) Continue until Vn, where n is the number of resolution bits

In this example, a SAR logic was used. A tracking ADC works in a similar way, but instead of doing a binary search, it increases or reduces the output of the DAC by one quantization step each time. In many cases, this has undesired converter characteristics, such as having a variable conversion time. Also, a tracking ADC is in general expected to be slower than a SAR ADC, although a more detailed analysis is needed, taking into account the type of signal to be converted and the settling time required for the comparator in both cases. Finally, sigma-delta ADCs are a promising option for this system, because sensors typically measure low-frequency physical parameters, and that is the realm of sigma-delta ADCs, but this alternative is more complex and it is not investigated in this work.

It is important to notice that the output code is a digital representation of the electrical parameter that acts as the controlling variable of the two-device sensor and not of the electrical parameter that is evaluated for equality. Sometimes the same sensor can be implemented by using either the voltage or the current as the controlling variable, which are the two options presented as ‘current mode’ and ‘voltage mode’ earlier. If only one of those electrical parameters provides meaningful information about the physical parameter, that one should be used as the controlling variable, such that its digital representation is obtained. For example, in the inverse Widlar sensor, since the gate voltage is proportional to the threshold voltage which carries the temperature parameter to be sensed, a voltage mode loop is desirable. On the other hand, in a PN junction PTAT generator, the current is the variable of interest, and it should be chosen as the controlling variable.

Controlling design parameters with the feedback loop

In Chapter 2, the design parameters were defined as those quantities that can be selected by the designer during the design time. Examples of those are device sizes and bias conditions. In the previous section, the purely analog error amplifier has been replaced by a mixed-signal error amplifier, and this opens the door to other options. The DAC of Figure 14 can be a traditional DAC with either voltage or current output, or it can represent a digital word controlling the size of a device, or the value of any component. In this sense, the design parameters can be understood as additional electrical parameters, since they can be easily controlled during operation time. This approach is followed on the design presented in Chapter 4. A similar example of controlling a design parameter can be found in [WangYT15].

CHAPTER 4

TEMPERATURE SENSOR DESIGN

4.1 The Inverse Widlar Temperature Sensor

As introduced in Chapter 2, the inverse Widlar temperature sensor is based on the presumed fact that the threshold voltage is a linear function of temperature as how it is modeled in the BSIM models [BSIM3v3]. Under that assumption, by using two devices with different threshold voltages, an output voltage proportional to temperature can be obtained.

The concept of two-device sensor offers a different approach to designing this circuit. First, the design conditions required for the circuit to work as a temperature sensor will be analyzed. Then, different structures will be derived, all of them providing an output linear with temperature. Finally, a new kind of temperature sensor is designed. This sensor has the advantage that it does not require a process with two levels of threshold voltage, thus allowing lower supply voltages and possibly improving matching. Also, it has an embedded Analog-to-Digital Conversion, with an output code that is linear with the temperature.

The device used for this types of sensor is a MOSFET, in strong inversion. For now, it is assumed that both the size and the threshold voltage are design parameters. According to the square law model, the expression is:

$$I = \frac{1}{2}\mu C_{ox} M (V - V_T)^2 \tag{4.1}$$

This equation corresponds to equation (2.36) of Chapter 2, where the sensitivity analysis is done. In this sensor the output voltage is expected to be a linear function of the

threshold voltage, and insensitive to mobility and gate capacitance. A sensitivity analysis gives:

$$\Delta \ln(I) = \frac{1}{\frac{1}{2}\mu C_{ox}}\bigg|_Q \Delta\left(\frac{1}{2}\mu C_{ox}\right) + 2\frac{1}{V - V_T}\bigg|_Q (\Delta V - \Delta V_T) \tag{4.2}$$

Two observations can be made. The first observation is that, the first term on the right side of equation (4.2) involves disturbance physical and process parameters (mobility and gate capacitance density) but not design parameter. This term can always be cancelled out in the proposed two-device sensor designs as shown in the multiplicative case in Chapter 2. (It is assumed here that the gate capacitances density for the two devices are the same, which may not be true if the devices are made with different gate oxide materials. It is also assumed that the mobility for the two devices are the same, which may not be exactly true according to the BSIM model [BSIM3v3]). A second observation is that, in order to have a sensor output voltage that is a function of the threshold voltage, the second term should not cancel out. This means that the percentage change in the gate over drive voltage has to be different in the two devices if the objective is to have a temperature sensor. It is interesting to notice that from the sensitivity analysis, it can be deduced not only which terms have to be equal between the two devices in order to cancel out undesired process parameters (in this case the mobility and the gate capacitance), but also it can be deduced which design parameters have to be different, to prevent the terms containing the desired information from canceling out. Because the threshold voltage contains information about the temperature, that term has to be kept, which leads to the following requirement:

$$\left.\frac{1}{V-V_T}\right|_Q^A \neq \left.\frac{1}{V-V_T}\right|_Q^B \tag{4.3}$$

In a traditional inverse Widlar sensor, this is achieved by requiring the threshold voltages to be different ($V_{TA} \neq V_{TB}$) [HeJun10, ZhaoC11, LeeSH11, ZhaoC13, WangYT13, WangYT15]. Then, the device equations can be written as:

$$\begin{cases} I = \frac{1}{2}\mu C_{ox} M_A (V - V_{TA})^2 \\ I = \frac{1}{2}\mu C_{ox} M_B (V - V_{TB})^2 \end{cases} \tag{4.4}$$

Assuming $V_{TB} > V_{TA}$, and calling $\chi = \sqrt{M_A/M_B} < 1$, the solution is:

$$V = \frac{V_{TB} - \chi V_{TA}}{1 - \chi} \tag{4.5}$$

According to the BSIM model [BSIM3v3], the threshold voltage can be modeled as a linear function of temperature (if the bulk-source voltage is zero). Then, if χ is constant with respect to temperature, the voltage given in equation (4.5) is also a linear function of temperature. A very simple block diagram of this sensor is shown in the next figure, along with a circuit level implementation. In both cases, a voltage mode feedback loop is used, where the error amplifier has current inputs:

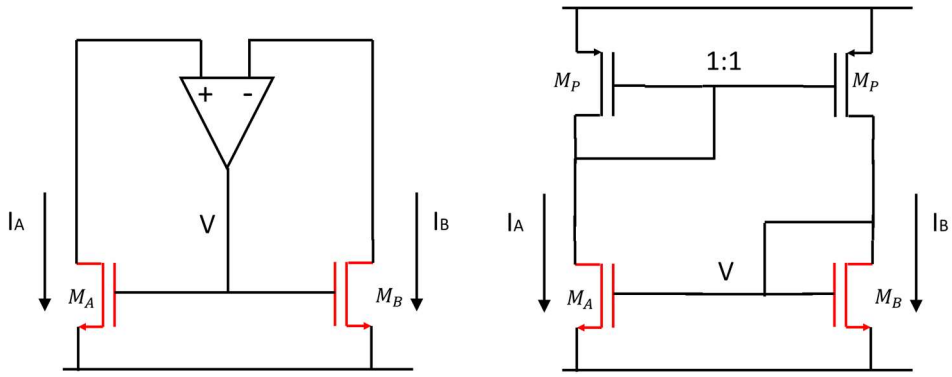

Figure 16 - Simplified diagram of an Inverse Widlar sensor and a simple circuit implementation

The circuit shown in Figure 16 is a very simple implementation that does not consider the impact of different drain-source voltages on the two devices M_A and M_B. This was neglected in the analysis, but the drain-source voltage is another electrical parameter that has to be controlled, to improve the matching of the devices. Cascoding the current amplifier is a way to control the drain-source voltage and also increase the gain of the error amplifier. The current of this circuit is not well controlled. It can be shown that it changes rapidly with temperature, and it also depends on process variations. Because of this, it is required that large design margins be used when sizing the components and choosing the biasing to take into account these variations and ensure the circuit works properly under various conditions. Finally, the circuit is self-bias and requires a startup circuit to guarantee the operating point is in the saturation region for all the transistors [WangYT12]. The startup circuit is not shown in the figure.

There are different ways in which different threshold voltages can be obtained in a given process. Some processes have low threshold voltage transistors for the core digital circuitry working at reduced supply voltages, and high threshold voltage transistors for power saving for higher supply voltages. If these options are not available, an equivalent transistor

can be built by stacking two regular transistors, as shown in Chapter 2. There are many issues with either option. Low-threshold voltage and high-threshold voltage transistors are not expected to match as well as two transistors of the same kind. The reason being that, in order to obtain different threshold values, the two transistors will go through different process steps. As will be shown later, mismatch has temperature dependency, and that could introduce nonlinearities in the output. Also, using two different threshold voltages requires higher supply voltage compared to the case where only low-threshold-voltage devices are used. The option of stacking two transistors to implement an equivalent high-threshold-voltage transistor increases the minimum supply voltage considerably, since the threshold voltage doubles and headroom for two gate-source voltages is needed. What is more, the stacked transistor is the device that needs the largest transconductance, then the area required for the stacked transistor is many times the area of the other device. Finally, the device that is on top requires a separate well to avoid threshold voltage modulation due to bulk-source voltage being non-zero. A separate well will increases the area required for the circuit and negatively impacts matching. If a separate well is not used, then the bulk-source voltage variation with temperature will introduce nonlinearities in temperature.

The above mentioned reasons explain why it is desirable to build an inverse Widlar sensor using two transistors of the same type with the same threshold voltage. They are expected to have better matching, allow lower supply voltages and consume less area. The following sections detail the design of this type of sensor.

4.2 Variations of the Inverse Widlar Sensor

Equation (4.3) asked for the derivative of the terms including the threshold voltage to be different on both devices. As shown before, the traditional approach uses different threshold voltages to satisfy this condition. If devices with the same threshold voltage are to be used, a new design parameter has to be introduced to force these terms to be different. The solution proposed is to attach a gain factor to the gate voltage of the MOSFET, as shown:

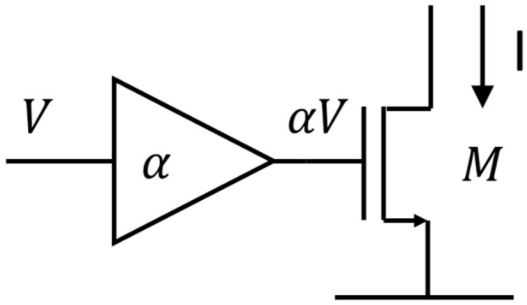

Figure 17 - Modified device for the inverse Widlar sensor

The device equation becomes:

$$I = \frac{1}{2}\mu C_{ox} M(\alpha V - V_T)^2 \tag{4.6}$$

Performing the differential analysis gives:

$$\Delta \ln(I) = \frac{1}{\frac{1}{2}\mu C_{ox}}\bigg|_Q \Delta\left(\frac{1}{2}\mu C_{ox}\right) + 2\frac{1}{\alpha V - V_T}\bigg|_Q (\alpha \Delta V - \Delta V_T) \tag{4.7}$$

In order for the two devices to keep the term including the threshold voltage, the design parameters $\alpha_A \neq \alpha_B$. The system of equations for this two-device sensor is:

$$\begin{cases} I = \frac{1}{2}\mu C_{ox} M_A (\alpha_A V - V_T)^2 \\ I = \frac{1}{2}\mu C_{ox} M_B (\alpha_B V - V_T)^2 \end{cases} \tag{4.8}$$

If $\chi = \sqrt{M_A/M_B} < 1$ and $\chi \cdot \alpha_A < \alpha_B < 1$, then:

$$V = V_T \frac{1-\chi}{\alpha_B - \chi \cdot \alpha_A} \tag{4.9}$$

For the particular case when $\alpha_A = 1$, a possible implementation is:

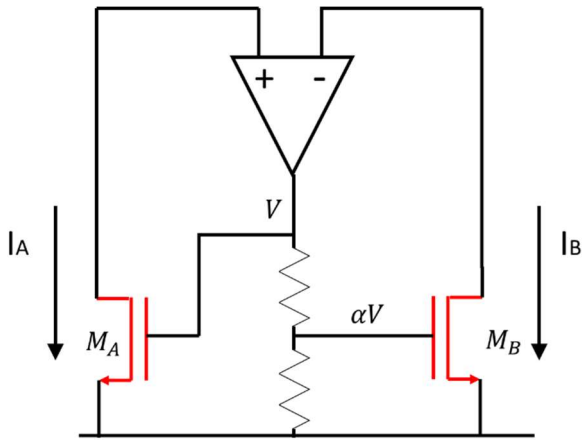

Figure 18 - The inverse Widlar sensor using MOSFETs with only one threshold voltage level

The circuit of Figure 18 is purely analog. In order to embedded Analog-to-Digital conversion in this two device sensor, the error amplifier can be replaced by the circuit introduced in Chapter 3. But, in this case, there is a better way to convert the error amplifier into a mixed-signal error amplifier. The design parameters α_A and α_B are gain/attenuation factors. Assuming $\alpha_A = 1$ and calling $\alpha_B \triangleq \alpha$, the equation (4.9) can be rewritten as:

$$V_{DAC} = \alpha \cdot V_{REF} = (1 - \chi) \cdot V_T + \chi \cdot V_{REF} \tag{4.10}$$

In equation (4.10), the variable under control of the feedback loop is no longer the voltage, but the attenuation factor α. This factor, multiplied by the reference voltage is nothing else but the output of a DAC, so the feedback loop senses the currents and adjusts the output of the DAC until the currents are equal. The output voltage of the DAC and its code are a linear function of the threshold voltage. A simplified model of the sensor is shown:

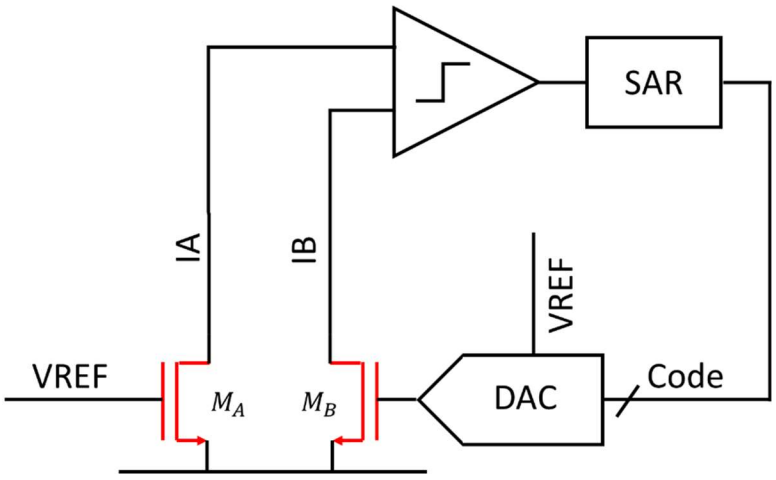

Figure 19 - Simplified model of temperature sensor with digital feedback

This circuit has a number of desirable properties: it uses only low-threshold-voltage devices; the output is a digital code that is a linear function of the threshold voltage, and the temperature; it does not need startup circuits, because the DAC can be designed to keep the gate voltage in the saturation region; and the current can be made almost constant with temperature variation, simplifying the design.

The analysis and design of this circuit are detailed in the remaining part of the chapter.

4.3 Idealized Circuit

In order to start the design, the properties of the transistors, such as threshold voltage at room temperature for different corners, variation of threshold voltage with temperature, and current levels are needed. To obtain these values, an idealized analog circuit is designed in Cadence. This idealized circuit has constant drain-source voltage for the transistors and ideal high gain error amplifier. It is shown in the next figure:

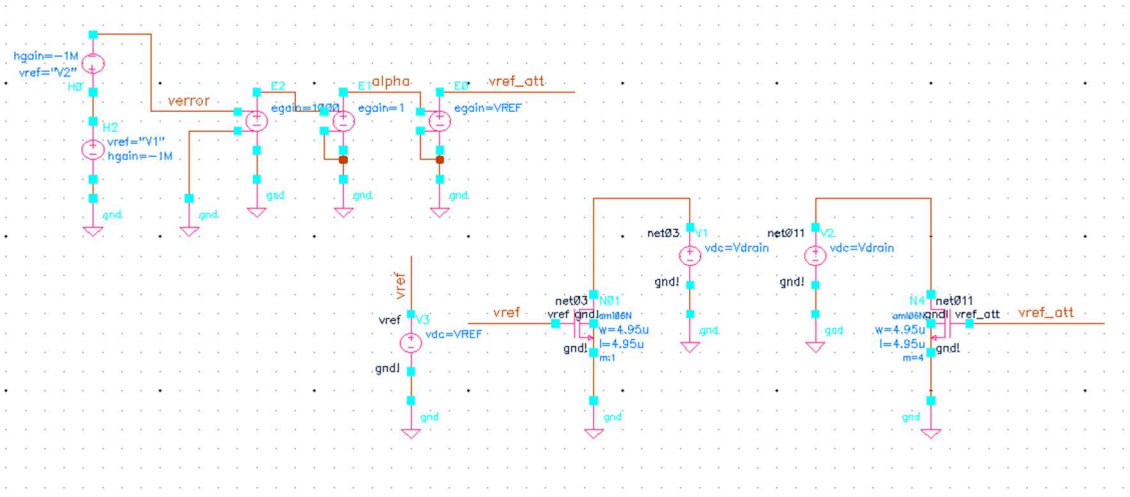

Figure 20 - Idealized sensor circuit

With the objective of reducing short channel effects, and also reducing the current consumption, the transistor lengths are chosen to be $L = 4.95\ \mu m$. The widths are also set to $W = 4.95\ \mu m$. The gate width affects the power consumption, the noise (both thermal and flicker noise), matching, and the gain of the sensor (that acts as a preamplifier for the comparator). Speed is not included in the consideration list, because it is not a limitation for a temperature sensor. Later on, some of these performance parameters are analyzed. Certainly, the sizing of the sensor is not critical, and other options are possible. It will be shown later that, in terms of matching and gain performance, these sizes do a good job.

The size ratio $\chi = \sqrt{M_A/M_B}$ is chosen to be one half, that is to say, device B is four times the size of device A. Part of the reason is because of the overdrive voltages of the devices. They are:

$$V_{ovA} = V_{REF} - V_T \tag{4.11}$$

$$V_{ovB} = \chi \cdot V_{ovA} \tag{4.12}$$

Reducing the ratio χ reduces the overdrive of device B, pushing it to moderate inversion. To avoid this, the overdrive of device A has to be increased, and then increase the reference voltage. Also, a small ratio consumes more area and makes the matching more difficult. A device ratio close to one, on the other hand, reduces the useful range of the DAC, and needs higher accuracy (in Volts) from the DAC.

From the idealized circuit of Figure 20, the threshold voltage of the devices with process and temperature variations are evaluated. The results are:

Table 1 - Threshold voltage variation (in mV) from idealized circuit

	NMOS/PMOS	Typical	SS	FF	SF	FS
Temp	0	756	795	719	800	723
	27	733	772	697	778	700
	50	714	753	677	759	681
	100	672	711	636	717	639

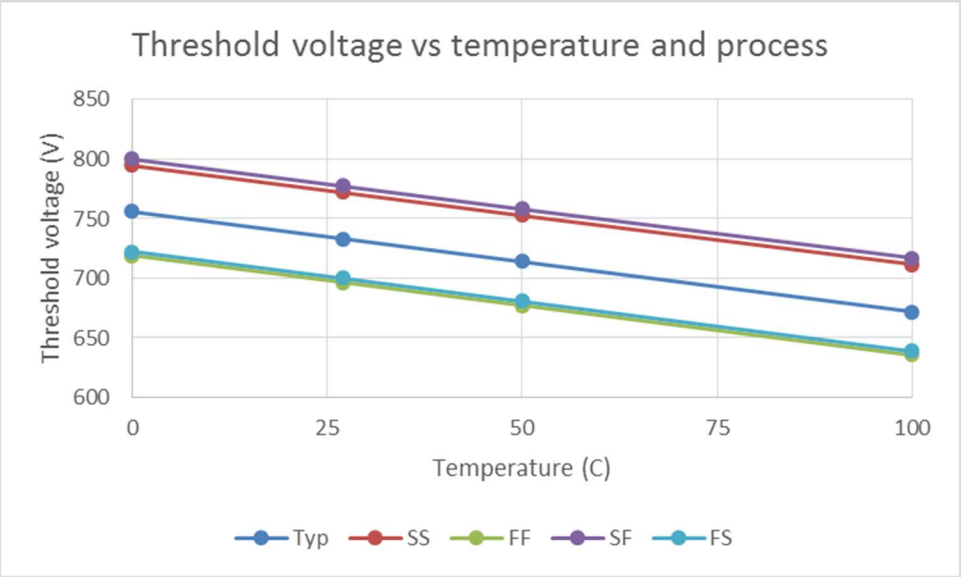

Figure 21 - Threshold voltage variation from idealized circuit

Figure 21 shows the reason behind this type of sensors. The threshold voltage, even though it suffers from process variations (and thus the sensor requires at least one-point calibration), shows a linear curve as a function of temperature.

From the maximum value taken by the threshold voltage, it can be decided the reference voltage:

$$V_{REF} > V_T^{MAX} = 0.8\,V \tag{4.13}$$

$$V_{ovB}^{MIN} = \chi(V_{REF} - V_T^{MAX}) > 200\,mV \tag{4.14}$$

It can be verified that $V_{REF} = 1.2\,V$ satisfies both requirements, and it is also a convenient value, being about the bandgap voltage. Another piece of information obtained from the simulation is the maximum overdrive voltage of device A:

$$V_{ovA}^{MAX} = V_{REF} - V_T^{MIN} = 570\,mV \tag{4.15}$$

In order to keep both devices in saturation, the drain-source voltage has to be higher than this value. For this design, it is assumed that the voltage of both devices is $V_{DS} = 0.7\,V$, set by cascoding.

Regarding the current, since the devices are biased with a reference voltage, Zero-temperature-coefficient (ZTC) biasing can be used [Filanovsky01]. This will not give constant current with respect to temperature, but it will reduce its variation, making the design of the current comparator much easier. For the parameters of the process of this design:

$$V_{ZTC} = V_{T0} + \frac{\alpha T_0}{\eta_\mu} = 0.714\,V + \frac{-0.8\frac{mV}{ºC}\,(273\,ºC + 50\,ºC)}{-1} = 0.97\,V \tag{4.16}$$

A reference voltage of $0.97\,V$ would give ZTC bias for the nominal corner. But ZTC bias is not too sensitive to variations on the bias voltage or process corners. In fact, the reference voltage of $1.2\,V$ still gives a very good result, as shown next:

Table 2 - Drain current variation (in µA) from idealized circuit

	NMOS/PMOS	Typ	SS	FF	SF	FS
Temp	0	8.8	7.4	10.1	7.3	9.9
	27	8.8	7.4	10.1	7.3	9.8
	50	8.8	7.5	10.1	7.4	9.8
	100	8.8	7.6	10.1	7.5	9.9

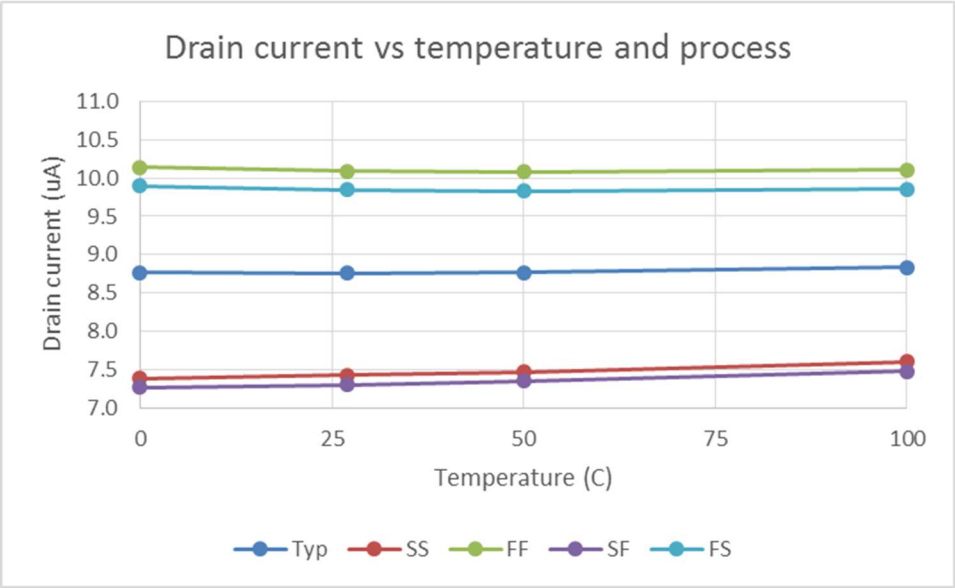

Figure 22 - Drain current variation from idealized circuit

As expected, the current suffers from process variation of about 30 %, which has to be absorbed by the current comparator, but it does not suffer from considerable temperature variations on top of those.

Finally, later on the transconductance of the device B will be useful. The simulation results with the idealized circuit are:

Table 3 - Transconductance variation (in μS) in the idealized circuit

	NMOS/PMOS	Typ	SS	FF	SF	FS
Temp	0	96	89	97	89	97
	27	92	85	94	85	93
	50	88	82	91	82	90
	100	82	76	85	76	85

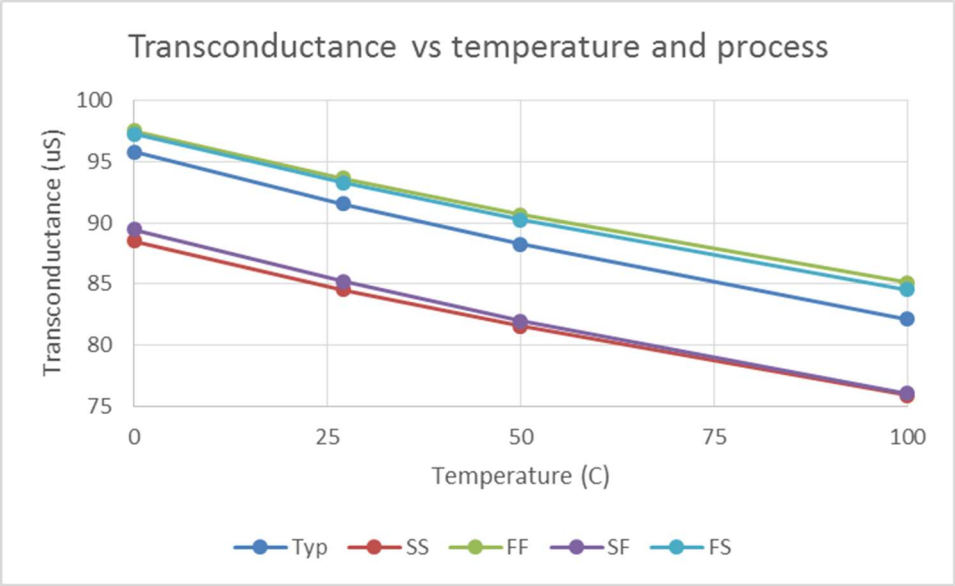

Figure 23 - Transconductance variation from idealized circuit

The transconductance is important because the device B can be understood as working as a preamplifier for the comparator.

The idealized circuit has the main components needed for the sensor: a current comparator, an idealized DAC, and voltage references for the drain-source voltage. In the next sections each block will be analyzed and designed, using the information provided in this section.

4.4 Linearity of idealized sensor

An important parameter of a comparator is its resolution, that is, the minimum input signal that will cause the comparator to produce either a definite zero or a definite one in the output. This value has to be small enough, such that an error in that decision will not affect the performance of the sensor. So, before moving into the design of the comparator, the performance of the sensor has to be analyzed. Ideally, the output code is linear with the threshold voltage, which in turn is linear with temperature. In the real case there are nonlinearities that make the slope of the output change with process corners and also make it to be a nonlinear function of temperature.

Using the idealized circuit, the output of the DAC is measured to obtain the following information:

- V_{DAC} range: Span of the output voltage of the DAC over all temperature range
- Sensitivity: Absolute value of the rate of change of output voltage with temperature
- Error 1-point cal / 2-point cal: Error of the output voltage, in degrees Celsius

Table 4 - Performance of the idealized circuit

	Min	Max	SS	FF	SF	FS	Typ
V_{DAC}_range (mV)	28.8	32.0	29.2	32.0	28.8	30.8	28.9
Sensitivity (µV/ºC)	288	320	292	320	288	308	289
error 1-point cal (ºC)	1.01	3.12	2.25	2.90	3.12	1.01	2.71
error 2-point cal (ºC)	0.05	0.69	0.57	0.05	0.69	0.14	0.51

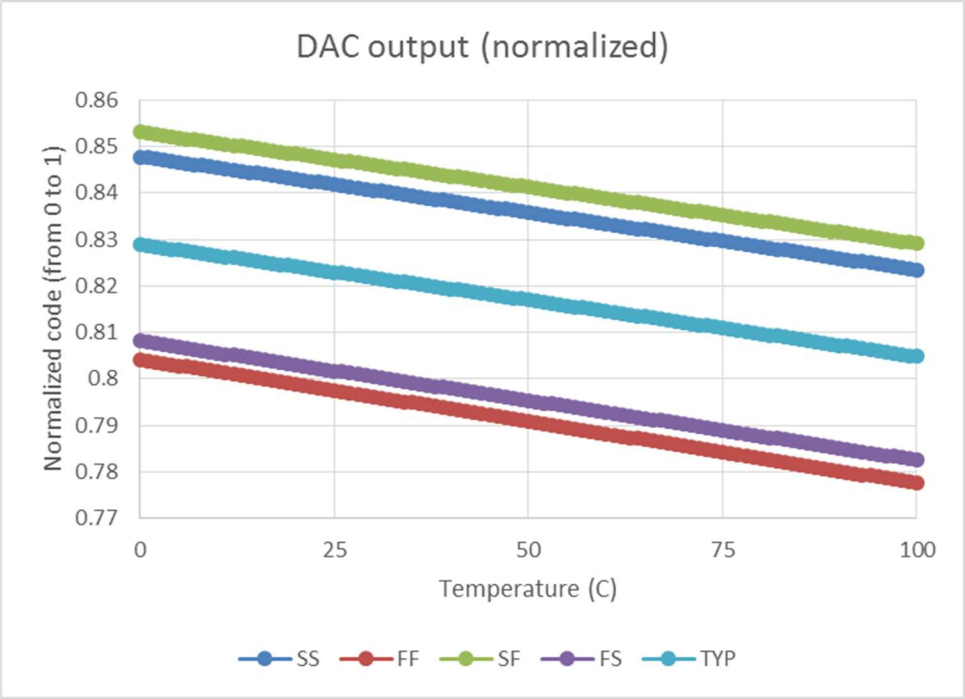

Figure 24 - Output code (normalized) of the idealized circuit

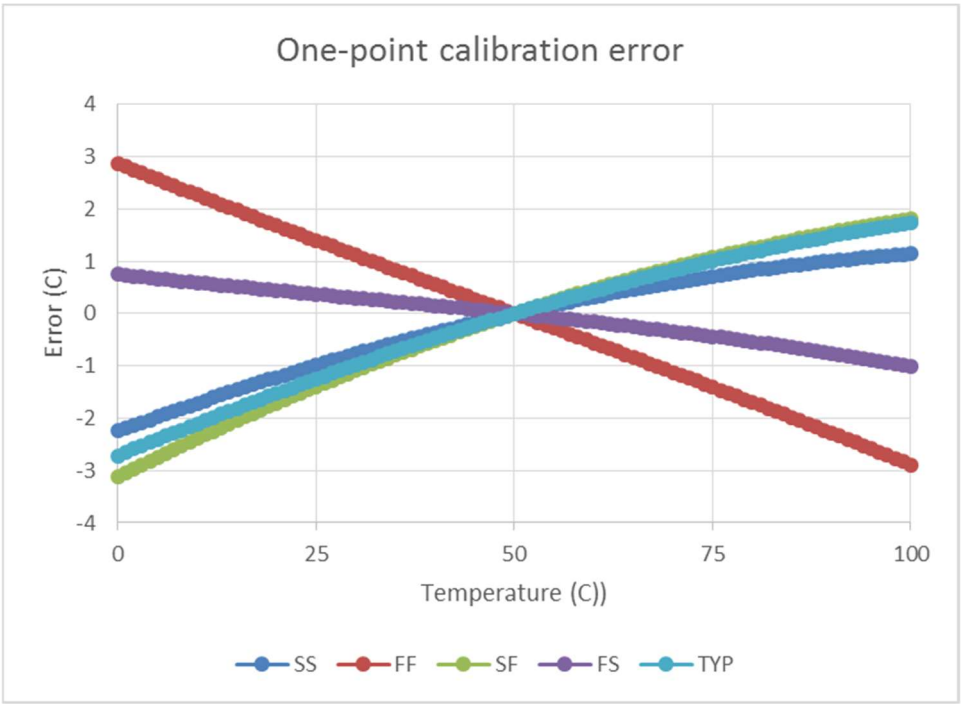

Figure 25 - Error after one-point calibration of idealized circuit

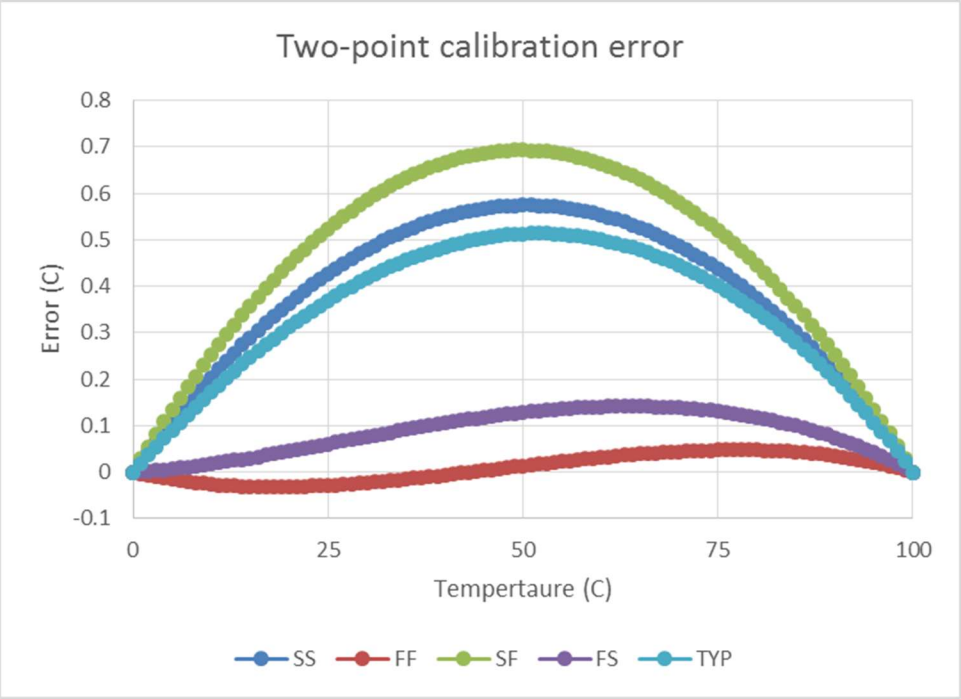

Figure 26 - Error after two-point calibration of idealized circuit

The accuracy, as equivalent number of bits, of the sensor can be defined as:

$$Accuracy \triangleq \log_2\left(\frac{Range}{Error_{MAX}}\right) \tag{4.17}$$

For one-point calibration the equivalent number of bits is 5 bits, while for two-point calibration it is 7.2 bits. The design detailed in this work is for the two-point calibration case. Both the comparator and the DAC have to be more accurate than 7.2 bits. Since the DAC range is about $30\,mV$, for an 8 bit DAC, the quantization step (V_{LSB}) is about $100\,\mu V$. From this analysis, the design conditions for the comparator and the DAC can be obtained.

4.5 Current Comparator Analysis and Design

Different options exist for a current comparator. One of the simplest circuits was shown before in Figure 16. The transresistance gain of that stage is low: just only the output resistance of a MOSFET. Another option is to use a folded cascode stage as a transresistance amplifier. This stage, in a single ended version, is shown next:

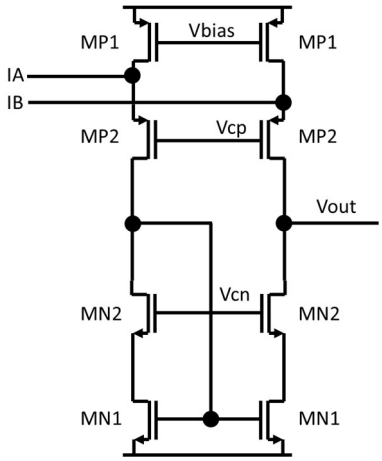

Figure 27 - Folded cascode stage working as current comparator

A fully differential stage can also be used. The advantage of a fully differential stage is that it does not have a systematic offset error, but it requires an active common-mode feedback circuit, which increases the complexity and power consumption.

A challenge with the structure of Figure 27 is that it has to absorb the common-mode current variations of the inputs. In the previous section, it was shown that, although the temperature variation is controlled by the ZTC bias, the process variation can be as large as 30%. In particular, a reduction in the input common-mode current produces an increase on the current of the folded cascode, and both effects produce a reduction in the gain of the stage. Thus, the gain of the stage also need to be overdesigned, to reach the minimum desired value over every corners. It is desirable that the bias current of the folded stage adjusts to the input

common-mode current. One way of achieving this is using a common-mode feedback loop controlling the PMOS current source. A better option, in this case, is to absorb the sensor core into the current mirror, as shown in the next figure:

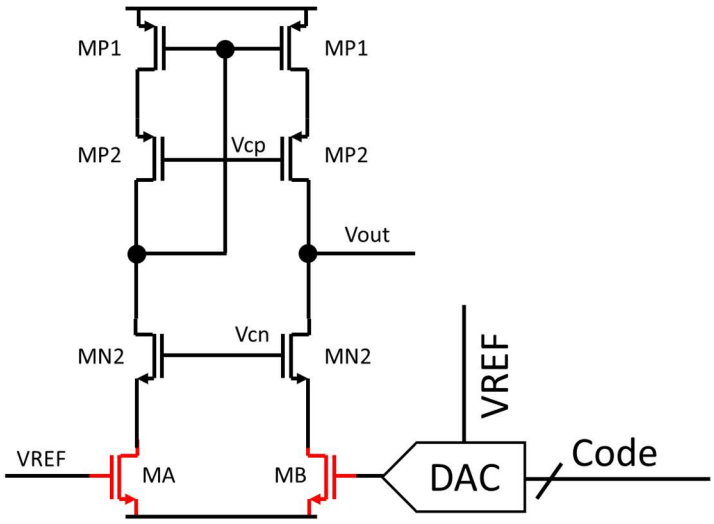

Figure 28 - Current comparator integrated into the sensor

In this circuit, the NMOS transistors that form the core of the sensor are effectively biasing the current comparator. Not only the gain variation with process is expected to be less, but also saved is power. The next subsections analyze the small signal gain, bandwidth, and both systematic and random offset.

Comparator small signal analysis

Even though this circuit is a current comparator, once the NMOS transistors are placed at the bottom, it can be analyzed as a voltage amplifier. Notice that it is not a voltage comparator, because it does not detect the zero crossing of the differential gate voltages of the

devices A and B. It still compares the drain currents for equality, but it is driven by a gate voltage. The small signal equivalent circuit for the branch of the device B is:

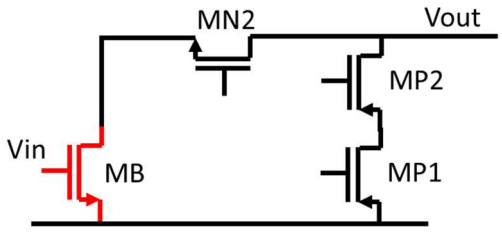

Figure 29 - Small signal equivalent circuit for the comparator

The PMOS transistors are an active load. They do not inject any signal, because the left branch of the circuit is quiet, from the feedback loop point of view. The output impedance of the PMOS side can be analyzed by means of the next circuit:

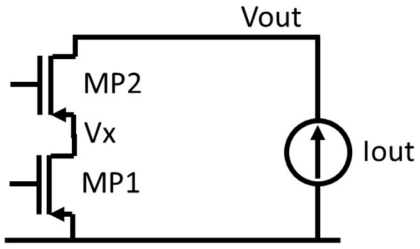

Figure 30 - Circuit to evaluate the output impedance of the PMOS side

The nodal equations are:

$$\begin{bmatrix} g_{ds2} & -g_{ds2} - g_{m2} \\ -g_{ds2} & g_{ds1} + g_{ds2} + g_{m2} \end{bmatrix} \begin{bmatrix} V_{OUT} \\ V_X \end{bmatrix} = \begin{bmatrix} I_{OUT} \\ 0 \end{bmatrix} \tag{4.18}$$

And the output resistance can be obtained:

$$r_{OUT} = \frac{1}{g_{ds1}} + \frac{1}{g_{ds2}} + \frac{g_{m2}}{g_{ds1} \cdot g_{ds2}} \tag{4.19}$$

From the NMOS side, the voltage gain can be obtained using the next simplified circuit:

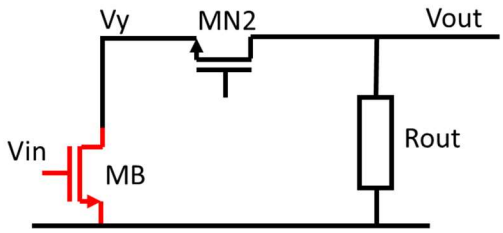

Figure 31 - Circuit to evaluate the voltage transfer function

The nodal equations for this circuit are:

$$\begin{bmatrix} g_{OUT} + g_{ds2} & -g_{ds2} - g_{m2} \\ -g_{ds2} & g_{dsB} + g_{ds2} + g_{m2} \end{bmatrix} \begin{bmatrix} V_{OUT} \\ V_Y \end{bmatrix} = \begin{bmatrix} 0 \\ I_{IN} \end{bmatrix} \tag{4.20}$$

Where device B's current is $I_{IN} = V_{IN} \cdot g_{mB}$. Solving for the transconductance:

$$\frac{V_{OUT}}{I_{IN}} = \frac{1}{1 + \frac{g_{dsB}}{g_{ds2}^N + g_{m2}^N}} \cdot \frac{1}{g_{OUT}^P + g_{OUT}^N} \cong \frac{1}{g_{OUT}^P + g_{OUT}^N} \tag{4.21}$$

Where g_{OUT}^N has the same expression as derived before for $g_{OUT}^P = 1/r_{OUT}^P$.

The first term of expression (4.21) represents the conductance current divider, that splits the input current between g_{dsB} and the current flowing through M_{N2}. Provided $g_{m2}^{N} \gg g_{dsB}$, it can be neglected, and obtain the transresistance of the stage as the parallel connection of the output resistances of the NMOS and PMOS side. The voltage gain of the stage can be written as:

$$\frac{V_{OUT}}{V_{DAC}} = \frac{-g_{mB}}{g_{OUT}^{P} + g_{OUT}^{N}} \tag{4.22}$$

It is useful, for the design procedure, to use quantities that are easily controllable. One of such quantities is the "intrinsic gain" of a MOSFET, defined as:

$$A_V^{(X)} = \frac{g_{mX}}{g_{dsX}} \tag{4.23}$$

If the intrinsic gain of the cascode devices is kept high, the output resistance can be approximated as:

$$r_{OUT} = \frac{g_{ds1} + g_{ds2} + g_{m2}}{g_{ds1} \cdot g_{ds2}} \cong \frac{A_V^{(2)}}{g_{ds1}} \tag{4.24}$$

Using the previous result, the gain of the comparator can be written as:

$$\frac{V_{OUT}}{V_{DAC}} \cong \frac{-g_{mB}}{\frac{g_{ds1P}}{A_V^{(2P)}} + \frac{g_{dsB}}{A_V^{(2N)}}} = \frac{-1}{\frac{1}{A_V^{(1P)} A_V^{(2P)}} \frac{g_{m1P}/I_D}{g_{mB}/I_D} + \frac{1}{A_V^{(B)} A_V^{(2N)}}} \tag{4.25}$$

Notice that the expression was rearranged to be expressed in term of intrinsic gains and g_m/I_D terms, which can be conveniently defined and simulated for any region of operation of the transistors.

The question that remains to be answered is how large the gain has to be. From the linearity simulation the $V_{LSB} \cong 100\ \mu V$. The comparator should detect a change of $1\ V_{LSB}$. If an output voltage swing of 1 V is considered, then the gain has to be at least $80\ dB$. The strategy followed to size the devices is to assume that both sides will produce the same order of intrinsic gain, then, the voltage gain can be written as:

$$\frac{V_{OUT}}{V_{DAC}} \cong -\frac{1}{2} A_V^{(B)} A_V^{(2N)} \tag{4.26}$$

The size of the device B was already defined. Its intrinsic gain is in the range of $50\ dB$ over process and temperature variations. The cascode has to provide an extra $30\sim40\ dB$ of intrinsic gain, which is not too high, so a shorter transistor is used. The width is kept the same, to facilitate easy layout. The cascode size is $W_{cascN}/L_{cascN} = 5\mu m/1\mu m$, and the intrinsic gain is in the range of $38\sim40\ dB$, including process and temperature variation.

The PMOS side is sized in a similar way. It will be shown later that the PMOS current mirror has a large influence on the input referred random offset, and so it is desirable to have large overdrive voltages and, at the same time large area to reduce flicker noise. All of this would produce a mirror that requires a very large area. They are sized to be $W_{1P}/L_{1P} = 4 \cdot 4.95\ \mu m/1.95\ \mu m$, which gives a gain about $45\ dB$ and the input referred offset is acceptable, as detailed later. The cascodes are the same size. The next figure shows the final design:

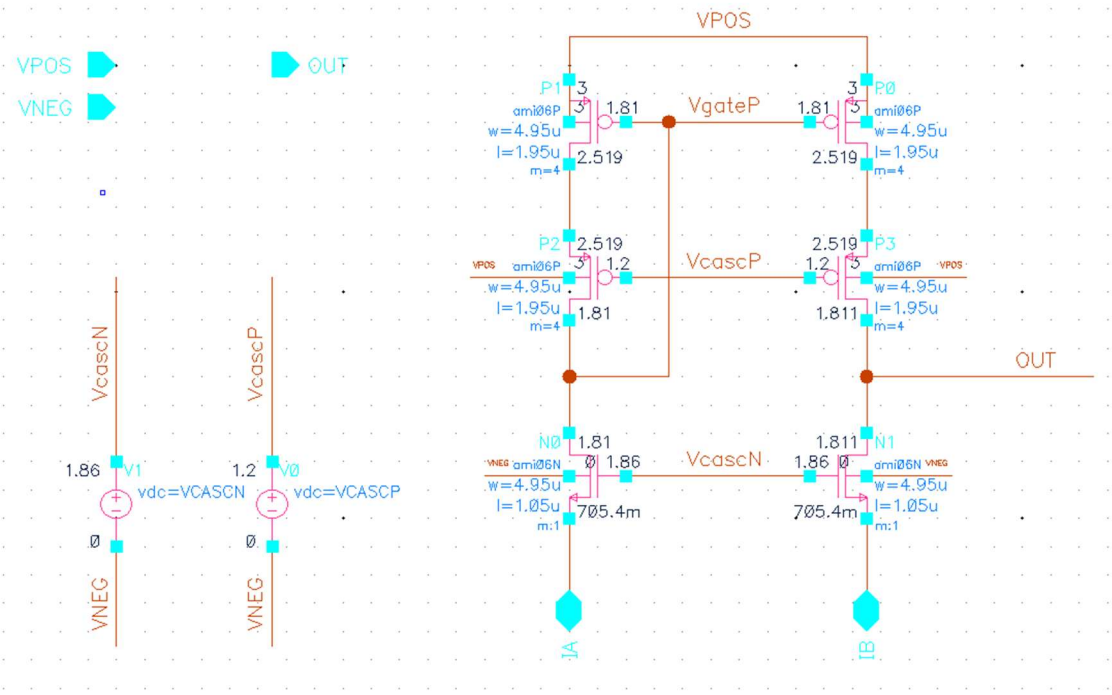

Figure 32 - Current comparator schematic

Regarding the cascode biasing, it can be self-biased or they can use an external reference. In this case, since a reference is already used, that is the option chosen. A self-bias structure would require a startup circuit to avoid the cascodes from taking the NMOS side to triode region.

To simulate the performance of the circuit, a replica bias is used. That is, one current comparator is closed loop, with an ideal feedback loop, working as an error amplifier. The gate voltage produced in this circuit (named Vreplica in the figure) is used to bias a second current comparator, which is open loop.

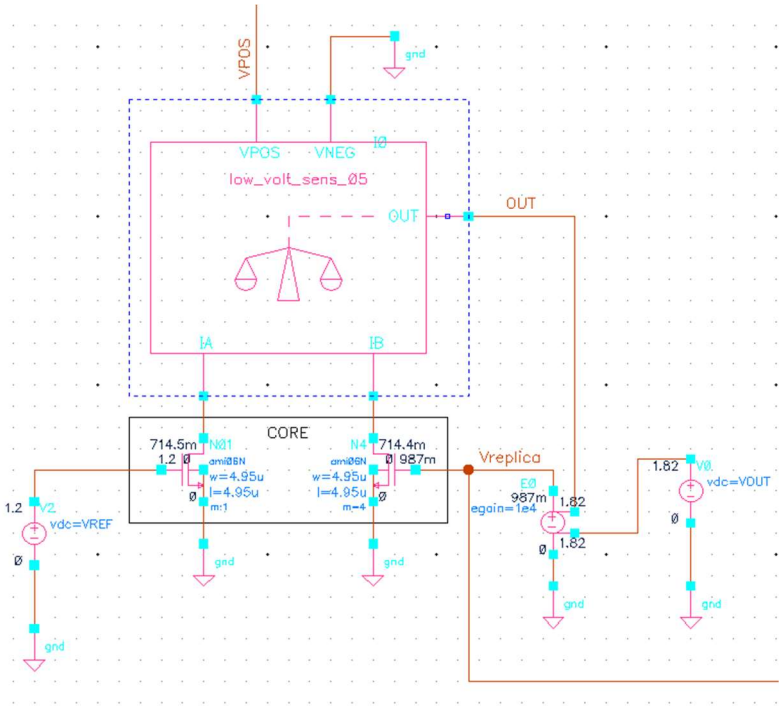

Figure 33 - Current comparator replica bias generator

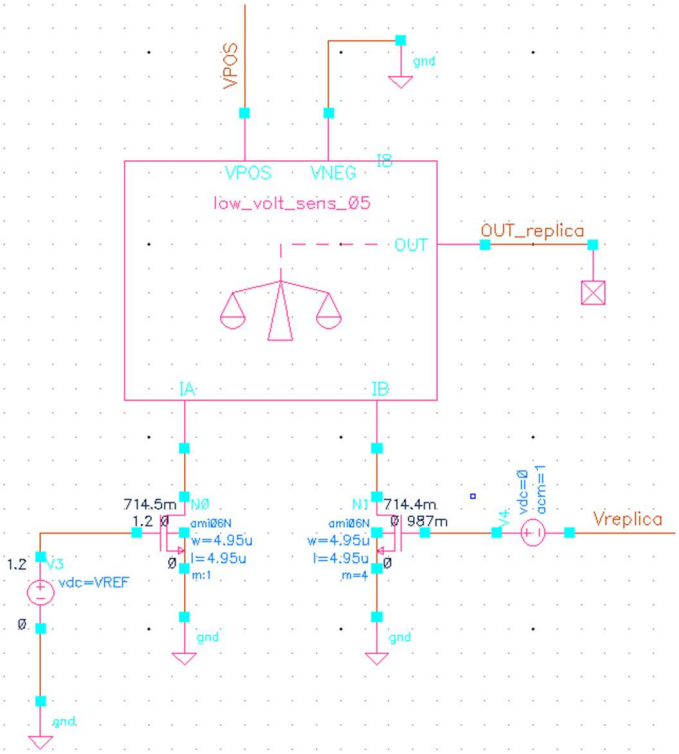

Figure 34 - Comparator testbench for small signal gain and bandwidth

The gain and bandwidth simulations give the following results:

Table 5 - Comparator gain (in dB) over process and temperature variations

	NMOS/PMOS	Typ	SS	FF	SF	FS
Temp	0	83.7	84.9	81.6	85.5	79.8
	27	83.2	84.4	81.2	85.0	79.4
	50	82.9	83.9	80.9	84.6	79.0
	100	82.1	83.0	80.3	83.7	78.1

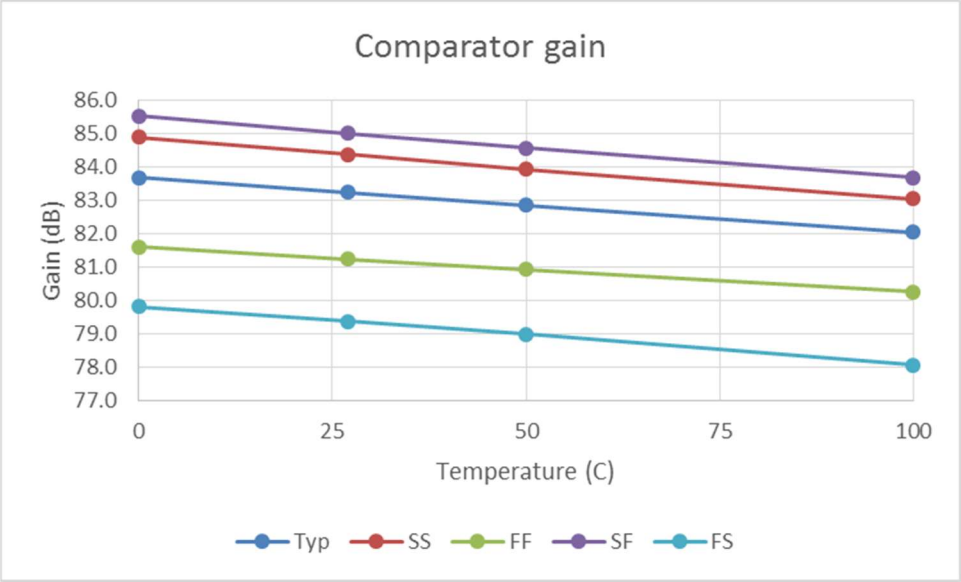

Figure 35 - Comparator gain over process and temperature variations

Table 6 - Comparator bandwidth (in kHz) over process and temperature variations

Bandwidth (kHz)

	NMOS/PMOS	Typ	SS	FF	SF	FS
Temp	0	30.0	23.9	38.5	22.7	46.9
	27	29.8	24.0	38.1	22.7	46.7
	50	29.8	24.1	37.9	22.8	47.0
	100	30.0	24.5	37.9	23.1	48.2

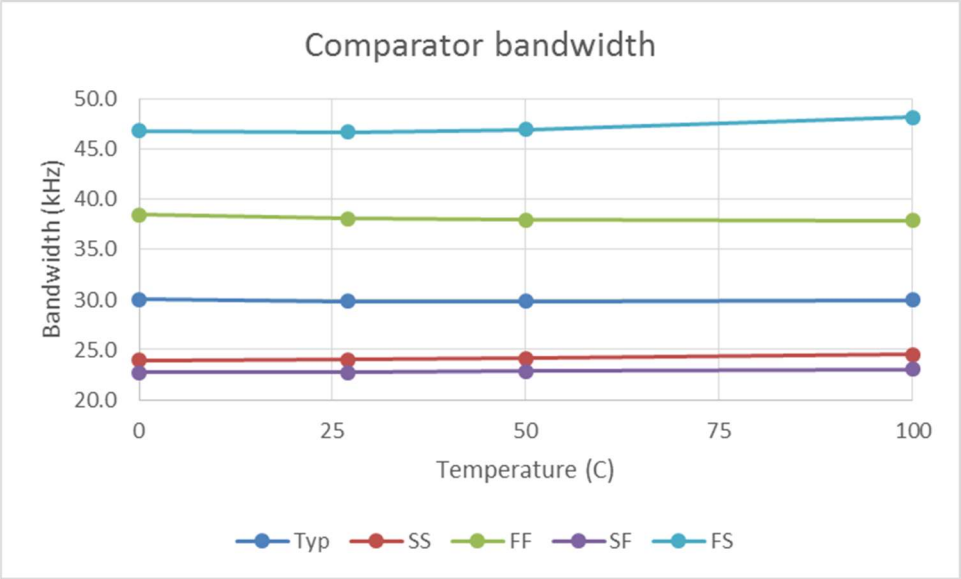

Figure 36 - Comparator bandwidth over process and temperature variations

The gain of the comparator is high enough for every corner. The worst-case bandwidth is slightly above 20 kHz, showing a one-pole response. Also, this comparator is not limited by slew-rate, because it drives a capacitance of a few femto Farads, and the current is in the range of micro Amperes. The time constant associated with this bandwidth is $\tau = 8\ \mu sec$. Since it is used in a SAR ADC, it has to settle to half the V_{LSB} of the ADC. Assuming a $n = 9\ bits$ ADC, the settling time of this comparator is approximately $t_{settling} = \tau\ (n+1)\ln(2) = 56\ \mu sec$, which gives a conversion time of $t_{conversion} = n \cdot t_{settling} = 500\ \mu sec$, or a sampling rate of $2\ kSamples/sec$. This sampling rate is high enough for temperature sensors, and it is limited by the low bandwidth of the comparator. There are good reasons to increase the speed of the comparator: increasing the speed of the conversion while keeping the sampling rate constant allows a reduction in power consumption, if the sensor is turned off when it is not doing any conversion. On the other hand, a fast comparator has multiple low gain stages, which increases the power consumption per stage.

Comparator systematic offset

A systematic offset is a shift in the switching point of a comparator due to asymmetries in the circuit. Fully differential structures are free from systematic offset because they are completely symmetric. On the other hand, single ended structures will introduce systematic offset. In many cases, it is useful to express the systematic offset as input-referred systematic offset. That is, an equivalent shift on the input referred switching point, as shown in the next figure:

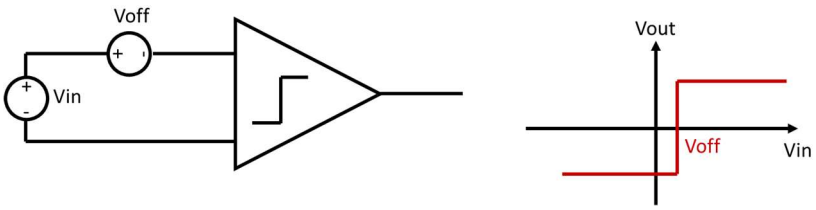

Figure 37 - Input-referred systematic offset

To test for systematic offset, the comparator's inputs are swept and the value that produces a change in the output is registered. Since the circuit is a current comparator, the testbench could be implemented as follows:

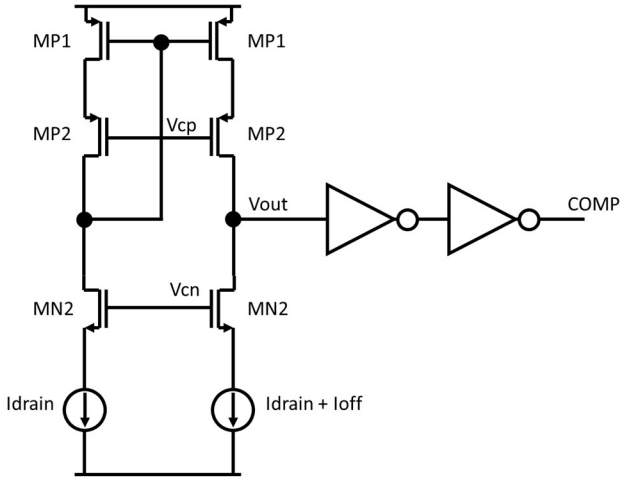

Figure 38 - Current comparator testbench with excessive gain

In Figure 38 the input currents are swept and the output signal COMP is observed. The inverters take the output of the comparator and give a well-defined logic value. The systematic offset is a result of the quiescent output voltage of the comparator being different than the threshold voltage of the inverter. First, define the quiescent output voltage as the voltage at the output when the inputs are equal:

$$V_{OUT}^{Q} \triangleq V_{OUT}|_{I_{off}=0} \tag{4.27}$$

This voltage is not, in general, the same as the inverter threshold voltage V_{INV}. The difference in these two values can be referred back to the input by dividing by the stage transresistance gain:

$$I_{off} = \frac{V_{OUT}^{Q} - V_{INV}}{r_{OUT}^{N}||r_{OUT}^{P}} \tag{4.28}$$

Equation (4.28) shows the problem with this testbench. The resistance r_{OUT}^{N} is many times higher than in the real circuit, as can be verified with equation (4.19). The problem is that the output impedance of the current sources is not a good representation of the actual output impedance of the NMOS transistors that bias the stage. This will overestimate the comparator gain and underestimate the input referred offset.

One way to overcome this problem is to use the NMOS transistors to bias the stage, as shown in the next figure:

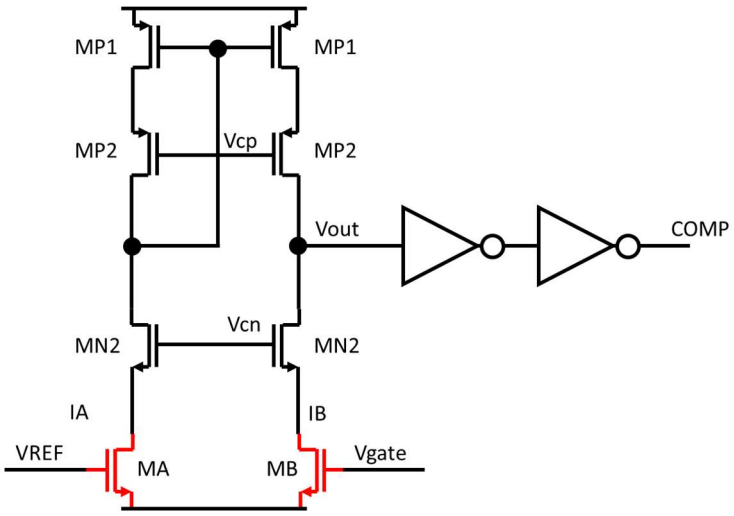

Figure 39 - Testbench for the comparator's systematic offset

It is important to notice that this circuit, even though it is now driven by voltage sources, it is still a current comparator. The way to simulate the input referred systematic offset is by defining two threshold voltages: $V_{gate}^{(I)}$ is the gate voltage for which $I_A = I_B$; $V_{gate}^{(V)}$ is the gate voltage for which the output of the comparator (COMP) changes. Based on these two values, that can be easily obtained, the input referred offset is calculated as:

$$Offset = V_{gate}^{(V)} - V_{gate}^{(I)} \tag{4.29}$$

The simulations give the following results:

Table 7 - Input referred systematic offset (in µV)

	NMOS/PMOS	Typ	SS	FF	SF	FS
Temp	0	21	19	24	20	31
	27	23	20	27	21	33
	50	25	22	28	23	36
	100	30	27	33	28	43
Variation (µV)		9	8	9	8	13

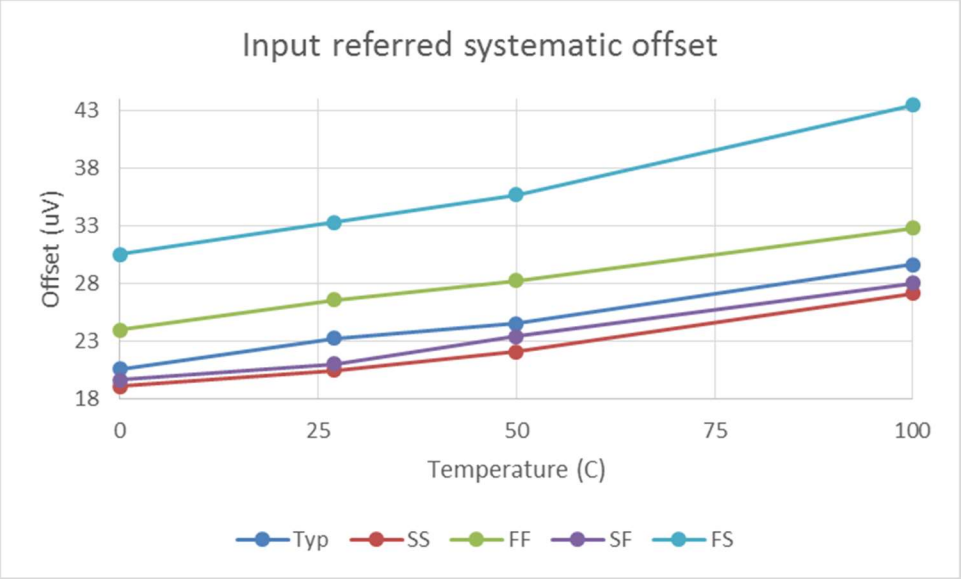

Figure 40 - Input referred systematic offset

In Table 7 the variation of the offset with temperature is also shown. The reason is that, since the sensor needs either one-point calibration or two-point calibration, a constant systematic offset would not affect its performance. Any input referred offset would be removed by the calibration. But the variation of the offset with temperature could introduce nonlinearities. Looking at the results of the simulation, the variation with temperature at any process corner is in the range of a few micro Volts, while $V_{LSB} \cong 100\ \mu V$. This means that the change across temperature is negligible even for the case of two-point calibration. What is more, a two-point calibration removes the linear component of the temperature variation, making it even smaller.

The previous analysis shows that, for this design, using a single-ended structure and having systematic offset is not a problem. In other situations, it might be, and a fully differential

structure would be needed. Without increasing the complexity of the circuit too much, a simple modification can reduce the input referred systematic offset:

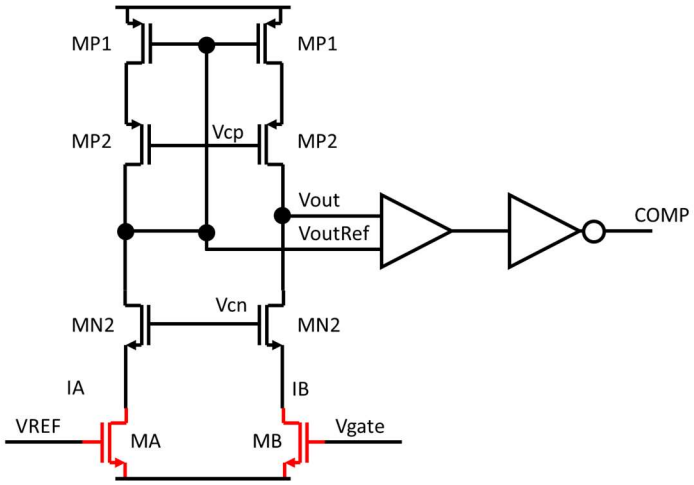

Figure 41 - Comparator with pseudo-differential output

This pseudo-differential output, followed by a differential stage, removes the error caused by the difference between the output quiescent voltage and the inverter threshold voltage. Actually, since at some point there will be an inverter, the input referred offset is improved by the extra gain introduced by the differential stage. For example, if the differential stage has a gain of 40 dB, the simulations of this pseudo-differential structure give an input referred offset less than 1 μV across process and temperature, with the resolution limited by the simulation setup.

Comparator random offset

Similarly to the systematic offset, a random offset that is constant across temperature would not introduce any error in a temperature sensor that is one or two-point calibrated. This analysis is concerned about the temperature variation of the input referred random offset. Since

the PDK used has no mismatch information on the model files, instead of running a mismatch simulation, the equations derived here are evaluated using simulated data.

MOSFET random mismatch is modeled by two independent Gaussian distributed random variables, both with zero mean [Laksh86, Pelgrom89, Drennan99, Drennan03]. These two variables are the threshold voltage mismatch and the relative current mismatch: $\Delta V_T \sim N\left(0, \sigma^2(\Delta V_T)\right)$, $\Delta\beta/\beta \sim N\left(0, \sigma^2(\Delta\beta/\beta)\right)$. Mismatch is a measurement of the difference between two devices that are designed to be identical. This definition of mismatch excludes device variations caused by so-called process variations which are typically large, and includes only device variations caused the local random variations in material or production processing. The standard deviation of the above mentioned two random variables are measured by the manufacturer, and are expressed as a function of the device size, as:

$$\sigma(\Delta V_T) = \frac{A_{V_T}}{\sqrt{WL}} \tag{4.30}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{4.31}$$

On each MOSFET, the effect of these two random variables can be explained as either an equivalent gate voltage or an equivalent drain current, as shown in the next figure:

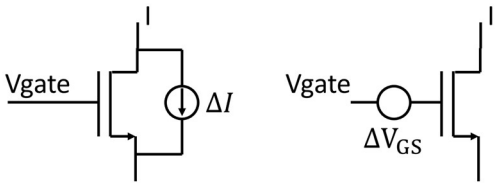

Figure 42 - Equivalent drain current source and gate voltage source to model random mismatch

These equivalent sources can be calculated (for the saturation region) as:

$$\frac{\Delta I}{I} = \frac{\Delta \beta}{\beta} - 2\frac{\Delta V_T}{V_{ov}} \tag{4.32}$$

$$\Delta V_{GS} = \Delta V_T - \frac{V_{ov}}{2}\frac{\Delta \beta}{\beta} \tag{4.33}$$

In this work, mainly due to lack of data, it is assumed that the fundamental random variables ΔV_T and $\Delta\beta/\beta$ are not a function of temperature. There are not many nor conclusive publications regarding this issue [Mennillo09, Andricciola09].

As mentioned before, this PDK does not include mismatch information on the device's cards, so the coefficients on equations (4.30) and (4.31) are estimated. Typically, the threshold voltage mismatch coefficient has a dependency on the oxide thickness, given by $A_{V_T} \cong 1\ mV \cdot \mu m \cdot t_{ox}/1\ nm$ for the NMOS, and 1.5 times larger for the PMOS. For a process with $t_{ox} = 13.5\ nm$, $A_{V_T}^{(N)} \cong 13.5\ mV \cdot \mu m$, and $A_{V_T}^{(P)} \cong 20.25\ mV \cdot \mu m$. The coefficient for the current mismatch does not have much variation across different processes, and a typical value is $A_\beta \cong 1\ \% \cdot \mu m$. These values are assumed for this process. Later on, it can be observed that small errors in the assumptions would not produce large differences in the results.

In order to simplify the analysis, only mismatch among the core NMOS transistors and the PMOS current mirror is considered. Any mismatch in the cascodes will translate as a mismatch in the drain-source voltage of the aforementioned NMOS's and PMOS's, but the channel length modulation affects the current by orders of magnitude below the gate-source

voltage level, and so does the mismatch affecting the drain-source voltage compared to the mismatch on the NMOS's and PMOS's. The simplified model for the sensor is shown next:

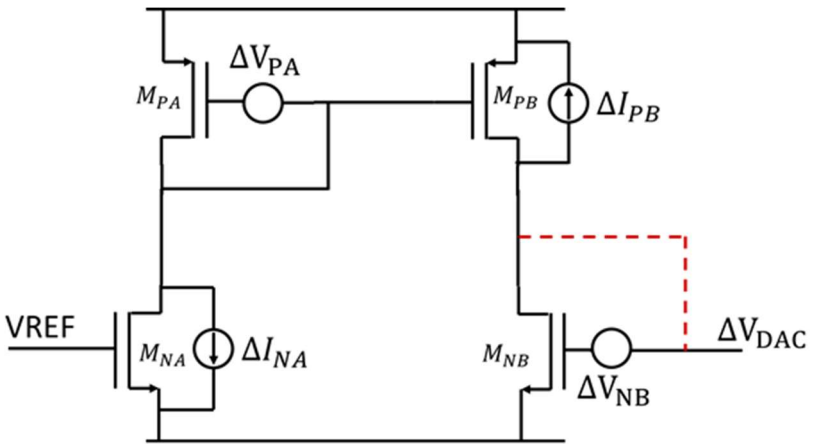

Figure 43 - Simplified sensor model to analyze mismatched-induced random error

In the model of Figure 43, the transistor M_{NB} is shown with a virtual diode connection. The reason is that, once the feedback settles, the gate voltage of that transistor adjusts to whatever the value is needed to let the drain current set by M_{NA} flow. This is, effectively, a diode connection. To be more precise, since the external feedback loop has gain, the diode connection has a loop gain that is higher than a regular diode connection, but this will not change the analysis. In the simplified model, each transistor's mismatch error is modeled with the voltage/current source that seems more convenient for the case. The objective is to obtain an expression for the random variable ΔV_{DAC}: the input referred error induced by the mismatch. Analyzing the circuit leads to:

$$\Delta V_{DAC} = \Delta V_{NB} + \frac{1}{g_{mB}}\left\{\Delta I_{PB} - g_{mP}\left[\Delta V_{PA} + \frac{1}{g_{mP}}\Delta I_{NA}\right]\right\} \tag{4.34}$$

This expression can be rearranged in a more traditional way, using the fact that a current referred error can be expressed as voltage referred and vice versa using: $\Delta I = g_m \cdot \Delta V$:

$$\Delta V_{DAC} = \Delta V_{NB} - \frac{g_{mA}}{g_{mB}}\Delta V_{NA} - \frac{I}{g_{mB}}\left(\frac{\Delta I_{PA}}{I} - \frac{\Delta I_{PB}}{I}\right) \tag{4.35}$$

The result from (4.35) resembles the input referred mismatch of a differential pair with an active load. The only difference being that the two transistors in the differential pair have different transconductance. In the case of a differential pair, the pair itself has a small overdrive voltage, in order to increase the g_m/I ratio. This will reduce the impact of the second term in (4.35). In a sensor, the NMOS devices are required to be in strong inversion, and thus the g_m/I ratio is small. The consequence is that the PMOS mirror has to be oversized to reduce the impact of its mismatch.

As stated before, the interest is not in the input referred offset, because it can be removed by calibration, but in the temperature variation of this offset. The expression (4.35) includes temperature dependent terms. They are made explicit in the next expression:

$$\begin{aligned}\Delta V_{DAC} = \Delta V_T^{(NB)} - \frac{V_{ov}^{(NB)}}{2}\frac{\Delta\beta}{\beta}^{(NB)} - \chi\left(\Delta V_T^{(NA)} - \frac{V_{ov}^{(NA)}}{2}\frac{\Delta\beta}{\beta}^{(NA)}\right) \\ + \frac{V_{ov}^{(NB)}}{2}\left(\frac{\Delta\beta}{\beta}^{(P1)} - \frac{\Delta\beta}{\beta}^{(P2)} - 2\frac{\Delta V_T^{(P1)}}{V_{ov}^{(P)}} + 2\frac{\Delta V_T^{(P2)}}{V_{ov}^{(P)}}\right)\end{aligned} \tag{4.36}$$

In this expression, $g_{mA}/g_{mB} = \chi$, $I/g_{mB} = V_{ov}^{(NB)}/2$, and the remaining terms have been replaced using (4.32) and (4.33). The standard deviations for each of these terms are summarized in the next table:

Table 8 - Mismatch error deviation

	Threshold voltage mismatch	Current mismatch
MNA	$\sigma\left(\Delta V_T^{(NA)}\right) = 2.73\ mV$	$\sigma\left(\frac{\Delta\beta}{\beta}^{(NA)}\right) = 0.2\ \%$
MNB	$\sigma\left(\Delta V_T^{(NB)}\right) = 1.36\ mV$	$\sigma\left(\frac{\Delta\beta}{\beta}^{(NB)}\right) = 0.1\ \%$
PMOS	$\sigma\left(\Delta V_T^{(P)}\right) = 3.26\ mV$	$\sigma\left(\frac{\Delta\beta}{\beta}^{(P)}\right) = 0.16\ \%$

The input referred offset has a standard deviation of about $5\ mV$, but more important than that is the temperature variation. The expression (4.36) represents a continuous time random process, where the variable is temperature. The only terms that have temperature dependency are the overdrive voltages. The expression (4.36) can be rearranged according to the temperature dependency:

$$\Delta V_{DAC} = \left\{\Delta V_T^{(NB)} - \chi \Delta V_T^{(NA)}\right\} + \frac{V_{ov}^{(NB)}}{2}\left\{-\frac{\Delta\beta^{(NB)}}{\beta} + \frac{\Delta\beta^{(P1)}}{\beta} - \frac{\Delta\beta^{(P2)}}{\beta}\right\} + \frac{V_{ov}^{(NA)}}{2}\left\{-\chi\frac{\Delta\beta^{(NA)}}{\beta}\right\} + \frac{V_{ov}^{(NB)}}{V_{ov}^{(P)}}\left\{-\Delta V_T^{(P1)} + \Delta V_T^{(P2)}\right\} \quad (4.37)$$

Each curly bracket in (4.37) includes a set of random variables that are not function of temperature. The first term is the input referred offset due to the threshold voltage mismatch of the NMOS transistors, and it is not a function of temperature at all. The next three terms have temperature dependency introduced by the functions they are multiplied to. In order to evaluate the temperature dependency of the input referred offset ΔV_{DAC}, the three function are plotted. To make a fair comparison, they are scaled by the standard deviation of the random variable that multiplies them.

The term $\Delta V_{DAC}^{(I)} = \frac{V_{ov}^{(NA)}}{2}\sigma\left\{-\chi\frac{\Delta\beta^{(NA)}}{\beta}\right\}$:

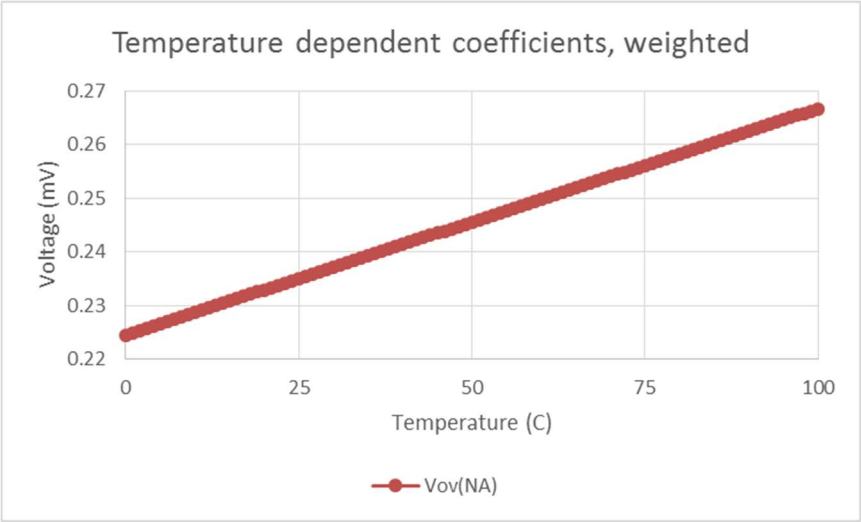

Figure 44 - Temperature dependency of first term of random offset

The term $\Delta V_{DAC}^{(II)} = \frac{V_{ov}^{(NB)}}{2}\sigma\left\{-\frac{\Delta\beta^{(NB)}}{\beta} + \frac{\Delta\beta^{(P1)}}{\beta} - \frac{\Delta\beta^{(P2)}}{\beta}\right\}$:

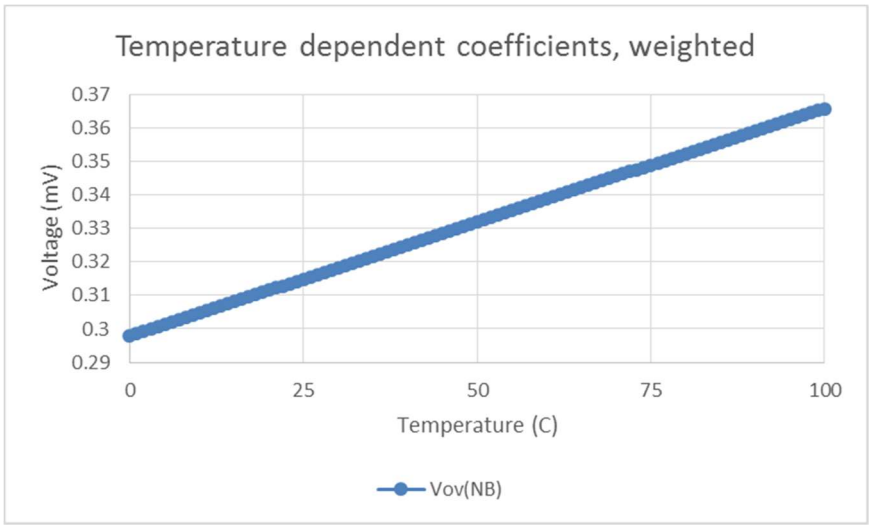

Figure 45 - Temperature dependency of second term of random offset

The term $\Delta V_{DAC}^{(III)} = \frac{V_{ov}^{(NB)}}{V_{ov}^{(P)}}\sigma\left\{-\Delta V_T^{(P1)} + \Delta V_T^{(P2)}\right\}$:

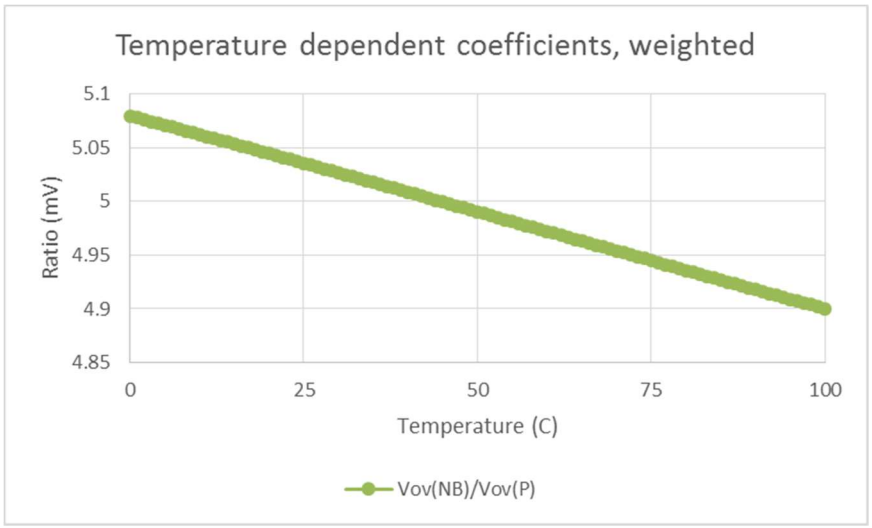

Figure 46 - Temperature dependency of third term of random offset

For every possible outcome of the different random variables in (4.37), the input referred offset ΔV_{DAC} can be expressed as a linear combination of the three functions analyzed before and a constant term, as shown:

$$\begin{aligned}\Delta V_{DAC}(\omega) = &\left\{\Delta V_T^{(NB)} - \chi \Delta V_T^{(NA)}\right\}(\omega) \\ &+ X_I(\omega) \cdot \Delta V_{DAC}^{(I)} \\ &+ X_{II}(\omega) \cdot \Delta V_{DAC}^{(II)} \\ &+ X_{III}(\omega) \cdot \Delta V_{DAC}^{(I)}\end{aligned} \tag{4.38}$$

where $X_i \sim N(0,1)$, independently distributed. If the three functions were linear functions of temperature, their linear combination also is, regardless of the value taken by the random variables. The figures seem to imply this. A more detailed analysis shows that $\Delta V_{DAC}^{(I)}$ and $\Delta V_{DAC}^{(II)}$ have a slope of $0.42\ \mu V/$ and $0.68\ \mu V/$ constant up to the second digit, and the third function $\Delta V_{DAC}^{(III)}$ has a slope of $-1.7 \sim -1.82\ \mu V/C$. Since the variables are Gaussians, in 99.7 % of the cases (three standard deviations apart), the slopes are at most three times these values either positive or negative. Two observations show that the input referred offset of this level will not affect the performance: 1) the functions are very linear, and most of their temperature dependency will be removed by a two-point calibration; 2) the slopes of these functions are small compared to the sensitivity of the sensor, which is about $300\ \mu V/C$. The change in the slope introduced by these functions has error effects below the 9 bit level, that is much less than the nonlinearity of the sensor itself.

4.6 Segmented DAC with Overlap

In a previous section, the accuracy of the sensor was evaluated, and it was shown to be 7.2 bits with two-point calibration. Also, under different corners, the sensor output spans a range about 30 mV. This is the range of voltages expected at the output of the DAC. But a regular DAC has an output that spans from 0 V to 1.2 V (the reference voltage in this design). In order to be accurate to the 7.2 bits level in a range of 30 mV, its resolution (and in-range accuracy) has to be at the 13 bits level. This is very expensive in terms of area. What is more, the actual problem is that not all the 0 V to 1.2 V range is used, which means that there is a way to reduce the requirements. There is a third reason why using that DAC would be a bad design: if the DAC is used in a SAR ADC, as in this work, during the binary search the output voltage could reach a value that puts the transistor outside the saturation region.

The proposed solution is to use a special type of segmented DAC. A segmented DAC has a division between the Most Significant Bits (MSBs) and the Least Significant Bits (LSBs), in such a way that different strategies can be used in the design of each of them. For example, the MSBs can be thermometer decoded, while the LSBs can be binary decoded. This reduces the complexity of the LSBs' decoder, while also reducing the Differential Non-Linearity errors (DNL) of the MSBs. The DAC used in this work is segmented and the MSBs are decoded in such a way that consecutive MSB codes increase by an amount that is less than the usual. This gives a DAC with overlap, where the same output voltage can be reached by different codes. An example of a DAC with overlap is shown in the next figure:

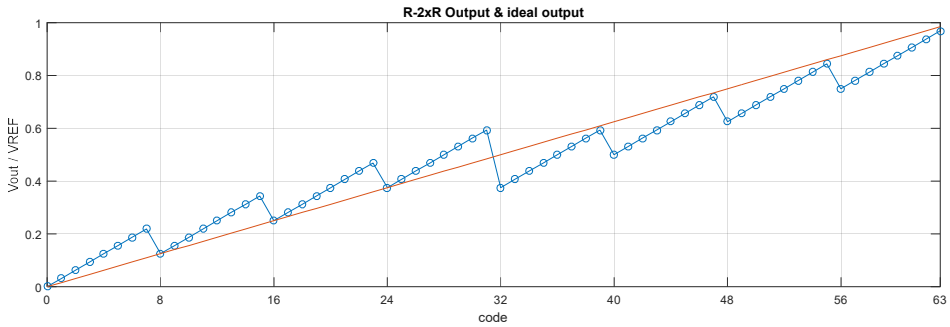

Figure 47 - Output voltage of a DAC with LSB = 3 bits, MSB = 2 + 1 bits

Figure 47 shows in blue the ideal output of a DAC with 3 bits of LSB, 2 bits of MSB and one extra bit. It can be noticed that consecutive segments have an overlap of one half. The reason is that the MSB step is reduced by half in this design. This also explains the need of an extra bit, to reach the upper half of the outputs.

Having overlap between the segments corresponding to each MSB is the reason why this segmented DAC can relax the accuracy requirement. The MSBs are allowed to have errors, because even with large errors, every output voltage can be reached. This means that this DAC is very robust against missing codes. More overlapping between consecutive segments relaxes the requirements on the MSBs more. The next figure shows the case of a segmented DAC with three quarters of overlap between consecutive segments. Since the overlap is more, more MSBs are needed, but with reduced accuracy requirement:

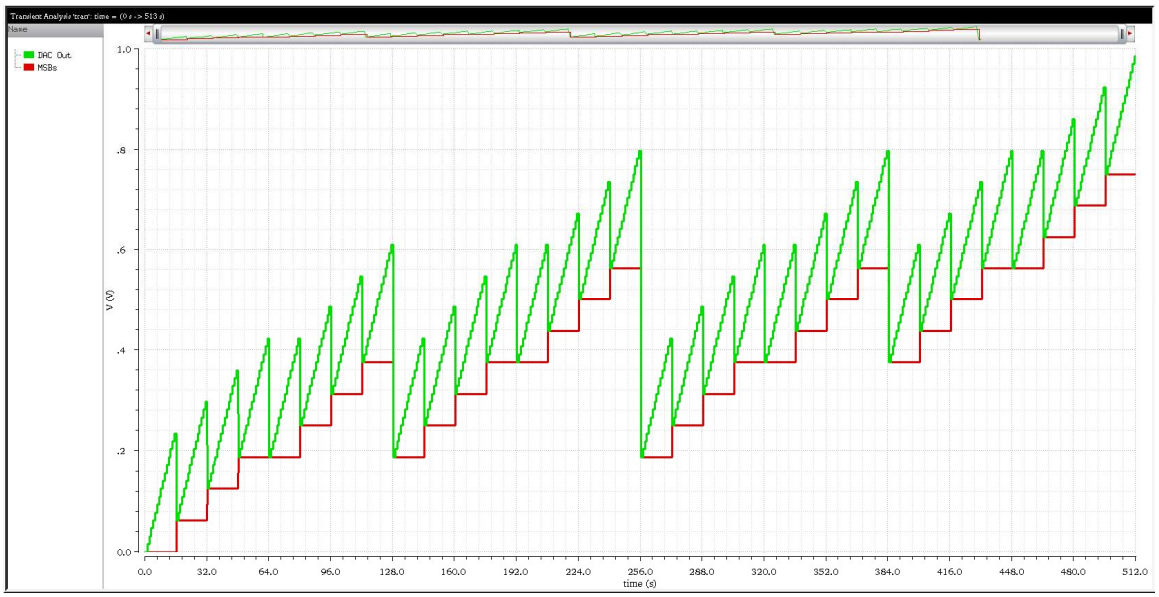

Figure 48 - Output voltage of a DAC with LSB = 4 bits, MSB = 2 + 3 bits (green). MSBs only (red)

Figure 48 shows the output of a DAC with three quarters of overlap between consecutive segments. It is also shown, in red, the output when the LSBs are kept at code zero. Notice how the MSBs increase by one quarter of the span of the LSBs. Also, it can be seen that there is not only overlap, but also many segments repeated. This is the result of the MSBs not being a binary scale, as it will be shown later.

Analysis of a DAC with overlap

The concept presented in the previous section can be implemented in different ways. In this case, a design based on a voltage-mode R-2R resistive DAC is presented. The R-2R DAC is a popular area-efficient way to implement a binary weighted resistive DAC, that avoids large resistor ratios. In general, the output of a binary weighted DAC can be expressed as:

$$\frac{V_{OUT}}{V_{REF}} = \sum_{i=0}^{n-1} \omega_i \cdot b_i \quad ; \quad \omega_i = \frac{1}{2^{n-i}} \tag{4.39}$$

A voltage-mode R-2R DAC of N bits is based on cascading N of the following unit cell:

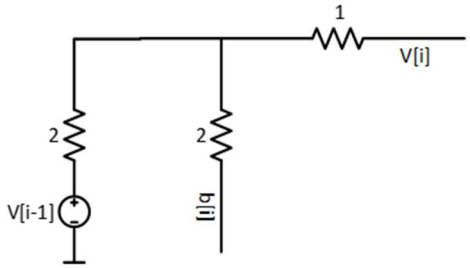

Figure 49 - Unit cell for a regular R-2R DAC

Since the output resistance (normalized, as shown in the figure) has a value of 2, the following recursive expression can be used to describe the R-2R:

$$\begin{cases} V_i = \frac{V_{i-1}}{2} + \frac{b_i}{2} \\ V_0 = \frac{b_0}{2} \end{cases} \tag{4.40}$$

For an N-bit DAC, the output is the voltage V_{N-1} of the expression from (4.40).

If the resistor connected to the input bit b_i is split, its weight is reduced, because the weight is proportional to the conductance of that resistor. For a DAC with overlap of one half, the MSBs weights should be reduced by half. It can be implemented with the following unit cell, used only for the MSBs:

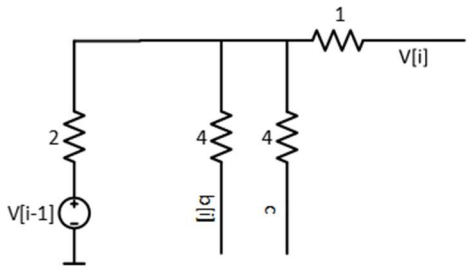

Figure 50 - Unit cell for the MSBs with overlap of one half

The expression that represents M-bits MSBs, is:

$$\begin{cases} V_i = \dfrac{V_{i-1}}{2} + \dfrac{b_i}{4} + \dfrac{c}{4} \\ V_0 = \dfrac{V_{LSB}}{2} + \dfrac{b_0}{4} + \dfrac{c}{4} \end{cases} \tag{4.41}$$

Note that in the recursive expression (4.41) the voltage V_0 represents the lowest MSB, and includes the voltage from the LSB segment. Also, a new bit called $'c'$ is introduced. This bit selects whether the output voltage is in the range $(0, V_{REF}/2)$, or $(V_{REF}/2\,, V_{REF})$, as shown in Figure 47.

The next figure shows how this segmented DAC can be implemented, including an LSB R-2R section with L bits, and an MSB R-2R with overlap section and M+1 bits. The total number of bits of this structure is $Bits = L + M + 1$.

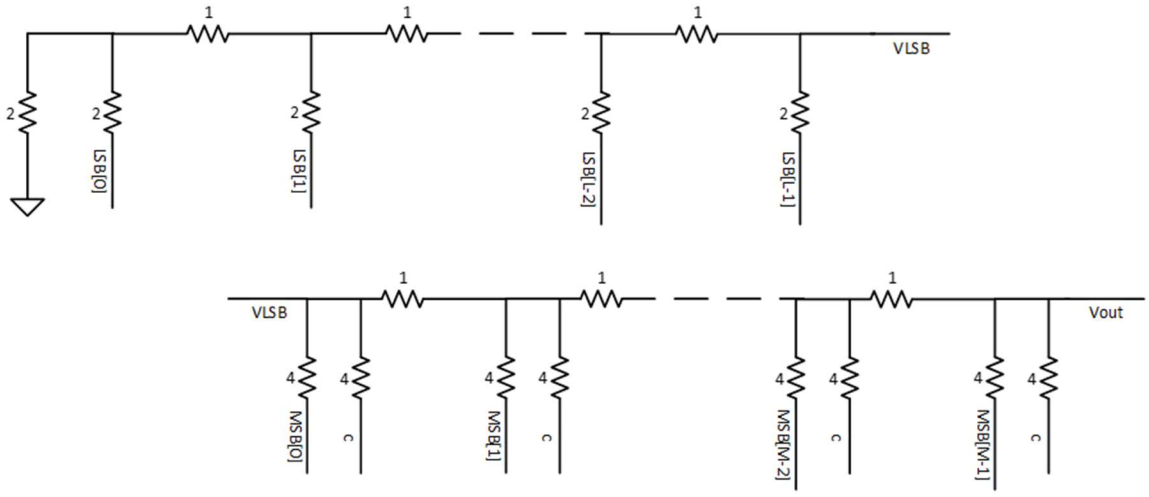

Figure 51 - DAC with overlap of one half, with L-bit LSB section and M+1-bit MSB section

A closed form expression can be easily derived from (4.40) and (4.41), but more insight can be gained by re-thinking the DAC using a signal flow diagram like the following:

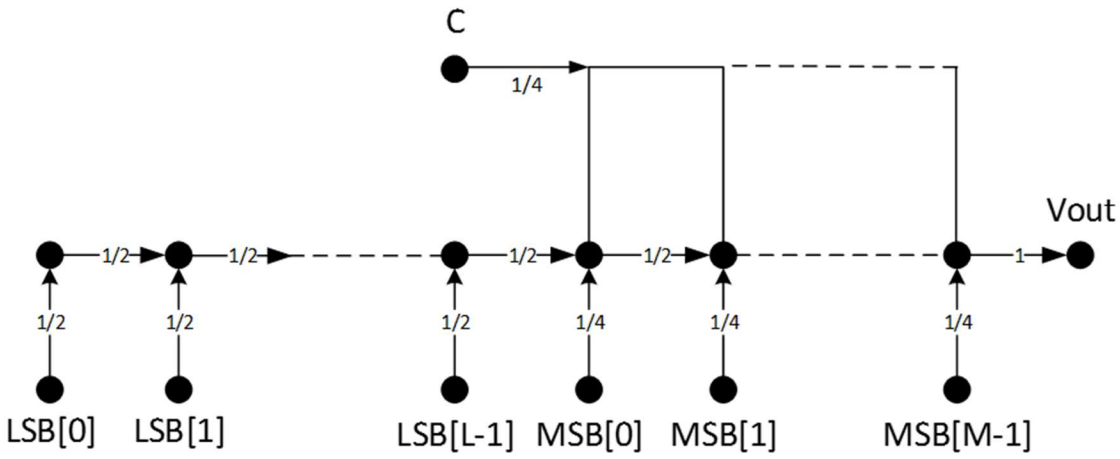

Figure 52 - Signal-flow diagram for the R-2R DAC with overlap of one half

As explained before, increasing the overlap of consecutive segments relaxes the accuracy requirement on individual resistors. The reason being that more error is allowed for a given code, as long as another segment still covers the same output range. There is a trade-

off between the overlap and the accuracy of the MSBs. A detailed analysis is out of the scope of this presentation. For an overlap of one half, it can be easily verified that the accuracy requirements on the resistors of the MSB DAC can be expressed in terms of the DNL. But when the overlap is three quarters or more, many segments are involved, and the accuracy requirements seem to be a function of the DNL of sets of consecutive codes, and not a single code.

Modifications for three quarters of overlap

In order to obtain three quarters of overlap, the resistors can be split once more, and reduce the weight by another half, as shown:

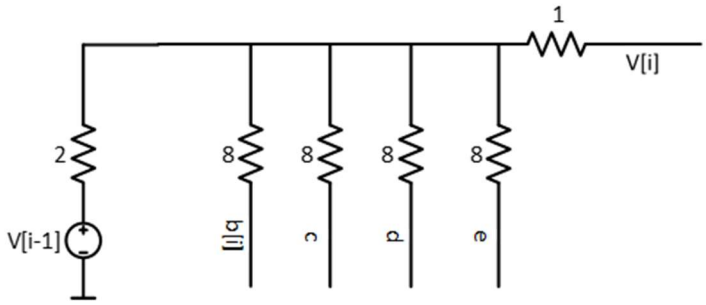

Figure 53 - Unit cell for the MSBs with overlap of three quarters

This unit cell would produce an output as shown in Figure 48. It can be seen that it has three extra bits, named $'c', 'd'$, and $'e'$. The fact that resistors with normalized values of 8 are needed seems contrary to the idea of keeping a small resistor ratio, as intended in the original R-2R. But two observations can be made: this structure has a reduced accuracy requirement, thanks to the overlap, and so the matching of the cell does not need to be so good; the cell can be modified to use resistors with values 1 and 2, as shown next:

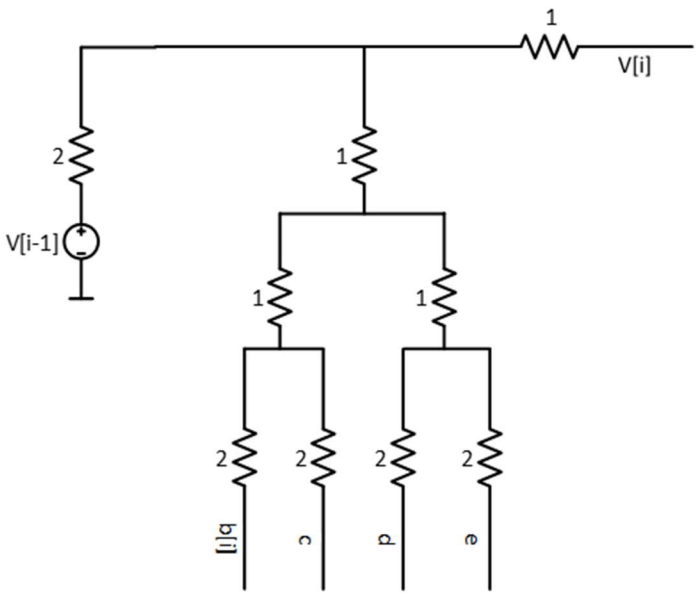

Figure 54 - Modified unit cell for the MSBs with overlap of three quarters

Design of the DAC with overlap

The operation of a DAC with overlap is as follows: the MSBs are adjusted during calibration: the code that corresponds to the segment that is better centered on the sensor's output is selected and fixed during the calibration. Then, during operation, the SAR logic controls only the LSBs. If a DAC with overlap of three quarters is considered, the total number of bits is $Bits = L + M + 3$. The range of output voltages reached by the LSBs (that is, the span) is:

$$Span_{LSB} = \frac{V_{REF}}{2^M} \tag{4.42}$$

The $Span_{LSB}$ has to be larger than the expected variation of the sensor across temperature. Not only to make sure that it will fit, but also because this is one of the reasons why the MSBs can have relaxed accuracy. In this design in order to keep the intrinsic accuracy of the sensor, the resolution of the LSBs is $L = 9\ bits$. The span is twice the expected output range of 30 mV. This gives $Span_{LSB} \cong 60\ mV$, which translates into $M = 4\ bits$. Notice how these two numbers still add up to 13 bit, but the accuracy of the LSBs is 9 bits, and not 13, while the MSBs are 4 bits and their accuracy is on that level, although a detailed analysis is needed.

The DAC is simulated and its transfer function is shown, for a reference of 1 V:

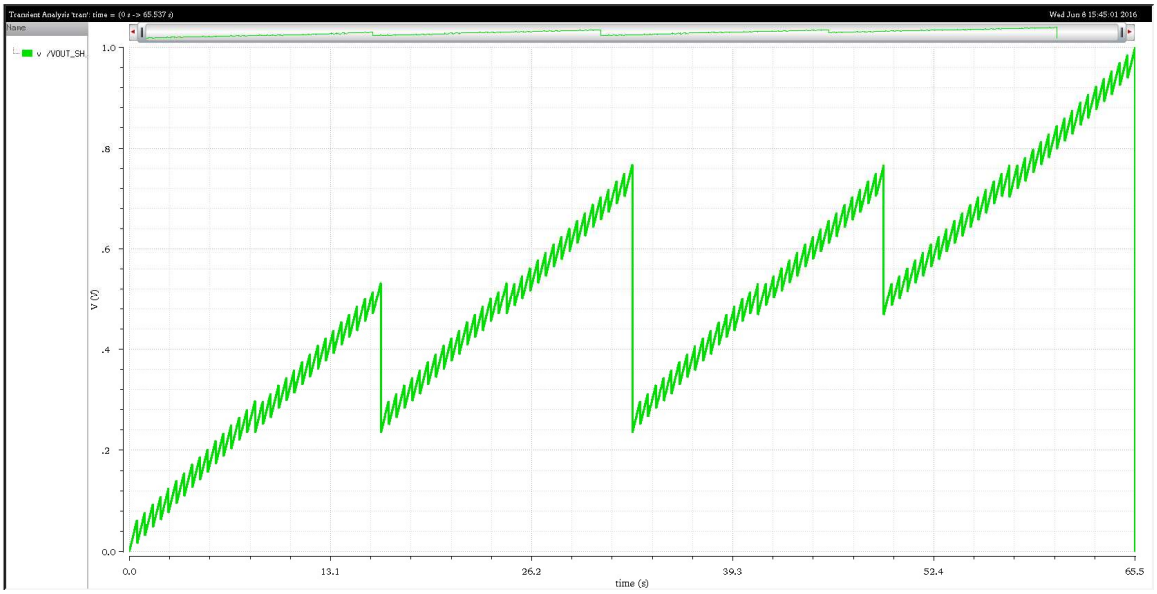

Figure 55 - Segmented DAC with 9-bit LSBs and 4+3 bits MSBs

Calibration procedure

Consider the case when the sensor is held at a temperature around 50 ºC (not necessarily accurate) in the testing plant. The output of the sensor is expected to be in the middle of its

output range, which is unknown due to process variations. The calibration equipment can find the proper MSB code for that part with a simple procedure: test the output code of the SAR ADC conversion for every MSB code. Most of them will saturate, and at least one is guaranteed to give a code close to the middle of the LSB scale. Any one of these MSB code is a suitable MSB code. This procedure can be made more efficient and fast, for example not testing codes that are known to fail, or doing a binary search. The important result is that the selection of the MSB does not need accurate measurements. After the MSB is selected, either a one-point or two-point calibration can be done, but it is only doing calibration of the LSBs, while the MSB bits are fixed.

To simulate the circuit, the first part of the calibration procedure can be mimic-ed by hand. From the idealized circuit, the output voltages of the sensor for different corners and temperatures can be obtained. They are shown in the next table:

Table 9 - Output voltages (in mV) of the idealized sensor across process corners and extreme temperatures

NMOS/PMOS	Typ	SS	FF	SF	FS
VDAC @ 0 ºC	994.7	1017.0	965.1	1024.0	969.8
VDAC @ 100 ºC	965.8	988.2	933.2	994.9	939.1

In the next figure, the expected voltage for a 0 ºC temperature is overlaid on top of the DAC's output.

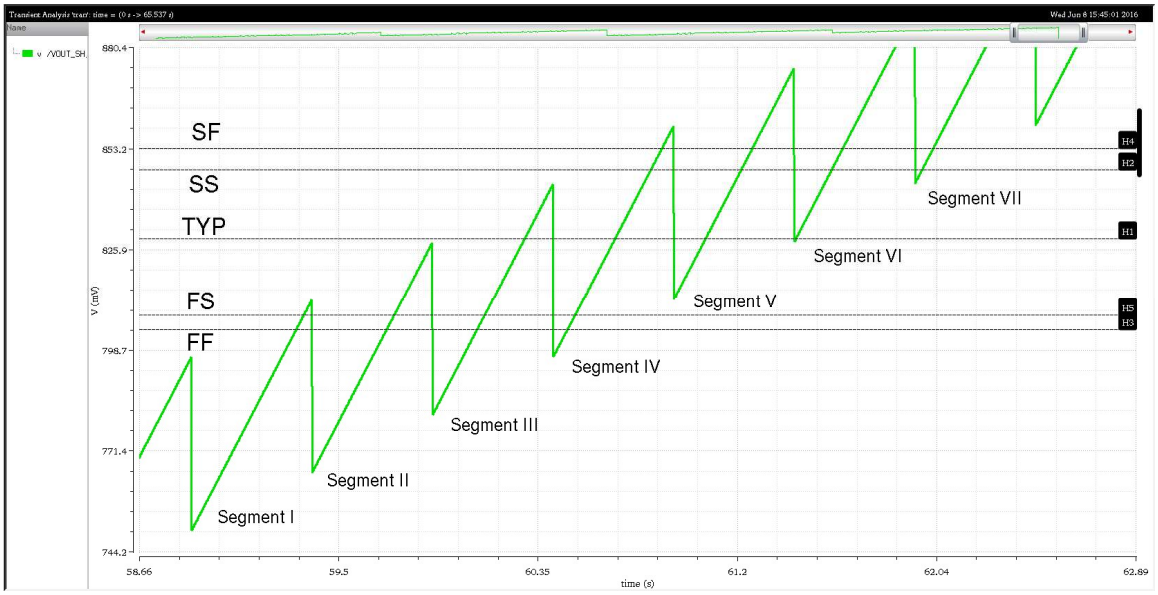

Figure 56 - DAC's output with horizontal lines showing the expected sensor voltage at 0 ºC

Each segment of Figure 56 corresponds to a different MSB code. It can be noticed that not every corner lie on the same segment. In order to do so, the segments would have to be increased, and correspondingly the resolution and accuracy of the LSBs.

Each horizontal line represents the 0 ºC output, which is the highest output for that corner. The calibration procedure detailed before would arrive to the conclusion that the optimum segments for each corner is:

Table 10 - Result of the simulated calibration procedure

Corner	Segment	MSB code
SF	5	111 - 0111
SS	5	111 - 0111
TYP	3	111 - 0101
FS	1	111 - 0011
FF	1	111 - 0011

In the next section, simulation results are presented. The codes from Table 10 are used as if they were obtained from the calibration procedure that selected the MSB segment.

4.7 Performance Simulation

The previous sections dealt with the design of each block in the system. A complete block diagram of the sensor is given in the figure below:

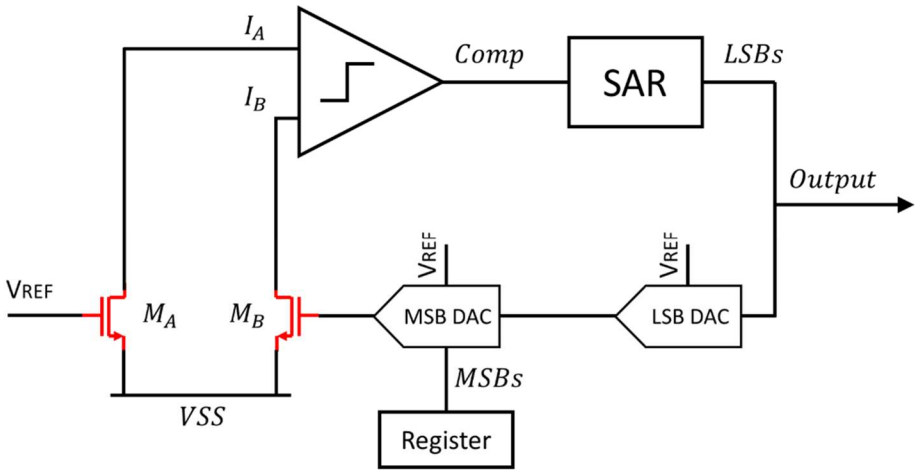

Figure 57 - Complete block diagram of the sensor

Simulation of this circuit consists of a transient analysis for one conversion cycle of the SAR logic. The clock frequency is set to $1kHz$, so a conversion takes 9 $msec$. Once the code for that temperature is obtained, the temperature is changed and the analysis repeated. The temperature sweep is from 0 $ºC$ to 100 $ºC$, in steps of 0.3 $ºC$. The output code is registered and both one-point calibration and end-point fit line are applied, to obtain the respective sensor errors. This procedure is repeated for every process corner.

A summary of the simulation is presented in the next table:

Table 11 - Simulation summary for the sensor

NMOS/PMOS		Typ	SS	FF	SF	FS
Code @ Temp.	0	390	289	444	332	476
	100	193	90	226	136	267
Segment		III	V	I	V	I
MSB code		111-0101	111-0111	111-0011	111-0111	111-0011
Sens (code/ºC)		1.97	1.99	2.18	1.96	2.09
Error 2-point cal (ºC)		0.70	0.60	0.39	0.79	0.35
Error 1-point cal (ºC)		2.58	2.13	3.20	3.11	1.32

The output codes for every corner are shown in the next figure. Notice that different corners might correspond to different MSB codes.

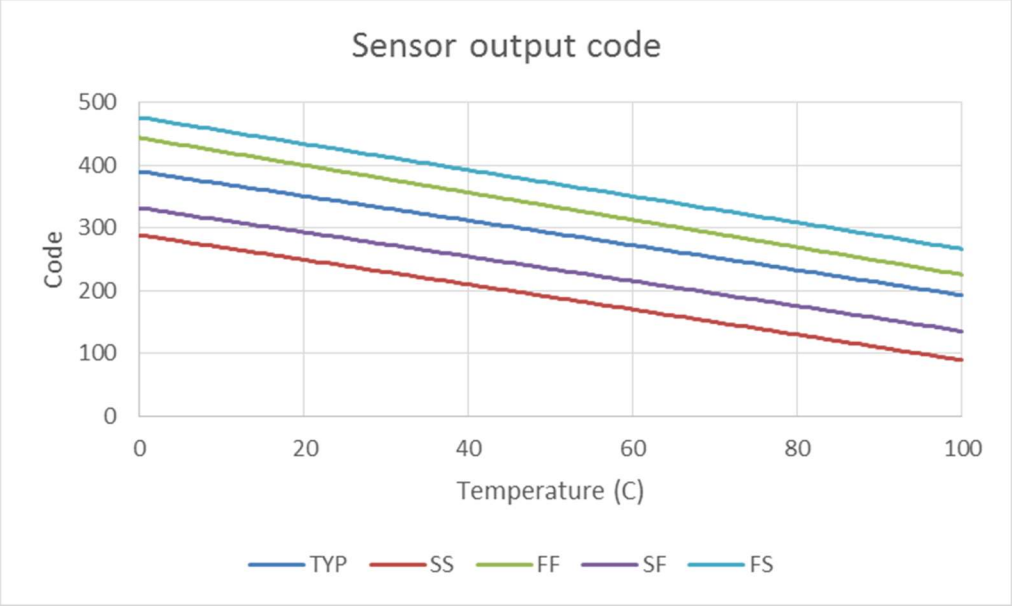

Figure 58 - Sensor output LSB code across temperature for different process corners

After one-point calibration, the worst-case error is 3.20 ^{o}C:

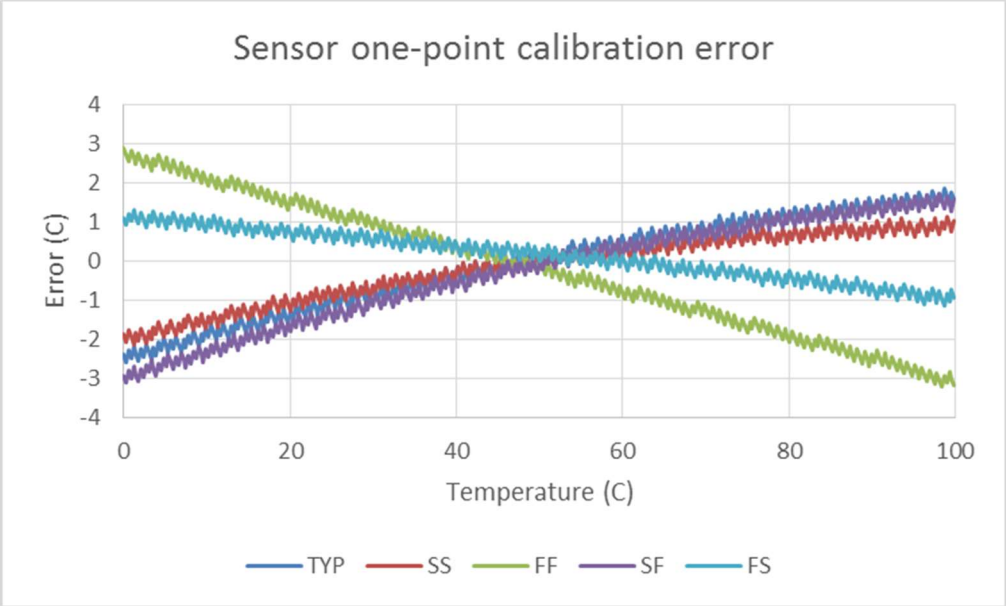

Figure 59 - Sensor error after one-point calibration

An end-point fit line gives a maximum error of 0.79 ^{o}C:

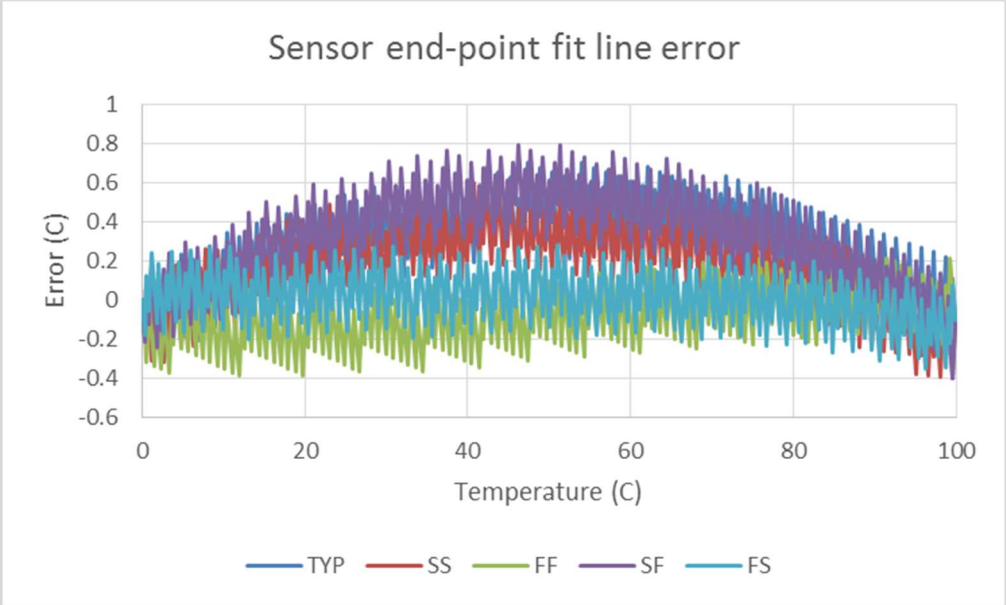

Figure 60 - Sensor error after end-point fit line

The results from Table 11 are compared with those obtained from the idealized sensor in Table 4, showing good agreement. It can be noticed that the end-point fit line error is slightly increased in the final sensor. This could be a consequence of some impact of the quantization error.

In conclusion, the modified version of the inverse Widlar circuit shows a performance that is equivalent to that of an idealized circuit, built with purely analog and ideal blocks, but adds analog-to-digital conversion and mechanisms to maintain the matching of the devices. The output is a linear function of the threshold voltage in the digital domain, which is an improvement over previous designs. The two-device sensor technique proves to be useful in gaining insight into the circuit behavior and in providing ways to modify it.

CHAPTER 5

SUMMARY AND CONCLUSIONS

The concept of two-device sensors with feedback enforced matching has been presented. It can be considered a systematic technique useful to analyze and design sensors and references. It has been shown that different common and important circuits can be understood as a circuit in the proposed framework. This helps to gain insight into their operation and, in some cases, to understand the modifications that would produce a performance improvement or other advantages.

Since a two-device sensor requires a feedback loop, different options to implement this loop are proposed. In particular, it would result in additional benefits to divide the design between the core of the sensor and the implementation of the feedback, because it gives flexibility in choosing them separately. Without an approach of this kind, the whole circuit would naturally be considered as a single block, making it more difficult to introduce modifications. A clear example of this advantage is the introduction of a feedback ADC to implement the feedback loop. This allows the sensor to have a digital output embedded. What is more, when the feedback is done in this way, the set of variables that can be controlled grows; not only voltages, currents, frequency, pulse width, or other typical electrical variables are possible: device sizes, component values and other type of design parameters can be dynamically adjusted.

As an application example, a variation of an Inverse Widlar temperature sensor has been designed. By means of the two-device sensor technique, this well-studied circuit was analyzed and modified. The benefits of this technique can be noticed in how simply variations

of the circuit can be obtained. In particular, the version of the sensor designed in this work overcomes the need of devices with different threshold voltage, and thus naturally improved matching. During the work, it has been shown that mismatch can be a strong source of nonlinearities. At the same time, this version of the circuit provides a digital output that is linear with temperature.

In conclusion, the technique presented in this work gives more and different kind of insight into self-biased circuits, and different types of references and sensors. It proposes ideas to improve references and sensors, and explains how to analyze and design circuits based on this method.

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